RISC-V

# Powering Embedded Computing with RISC-V SoCs

RISC-V is an open-source standard instruction set architecture (ISA) that is managed by the non-profit RISC-V Foundation. This modular ISA has a base instruction set and optional extension sets. Because RISC-V is free and open-source, it has gained popularity worldwide. Over 65 RISC-V cores, both commercial and open-source, are available today.

Efinix has created 3 RISC-V SoCs based on the VexRiscv core created by Charles Papon. The VexRiscv core, which won first place in the RISC-V SoftCPU contest in 2018, is a 32-bit CPU using the ISA RISCV32I with M and C extensions, has five pipeline stages (fetch, decode, execute, memory, and writeback), and a configurable feature set. Each SoC has a RISC-V processor, memory, a range of I/O, and interfaces for embedding user functions. You can easily create entire systems that include embedded compute and user-defined accelerators all in the same Trion® FPGA.

## Ruby SoC

Cached, high-performance SoC with a DDR DRAM controller interface.

Ideal for applications that provide real-time system controls and perform image signal processing.

- ~14K LEs/94 RAM blocks
- 50 MHz
- 1.16 DMIPS/MHz
- Up to 3.5 GB DDR DRAM
- 4 KB on-chip RAM
- 16 GPIO
- Timer
- PLIC
- 3 SPI masters
- 3 $I^2C$ masters/slaves
- 2 UARTs
- 1 AXI4 user peripheral
- 2 APB3 user peripherals

## Jade SoC

Cached, general-purpose SoC that blends performance with a smaller footprint.

Ideal for applications that use communications protocols, such as command and control, industrial automation or data logging.

- ~7K LEs/93 RAM blocks
- 50 MHz
- 1.2 DMIPS/MHz
- 32 KB on-chip RAM
- 16 GPIO
- Timer
- PLIC
- 2 SPI masters
- 2 $I^2C$ masters/slaves
- 1 UART
- 1 APB3 user peripheral

## Opal SoC

Cacheless, compact SoC with a small resource footprint.

Ideal for applications that require embedded compute capability such as system monitoring or remote configuration and control.

- ~5K LEs/16 RAM blocks
- 50 MHz/20 MHz
- 0.98 DMIPS/MHz
- 4 KB on-chip RAM
- 8 GPIO
- Timer
- PLIC
- 1 SPI master
- 1 $I^2C$ master/slave
- 1 UART
- 1 APB3 user peripheral

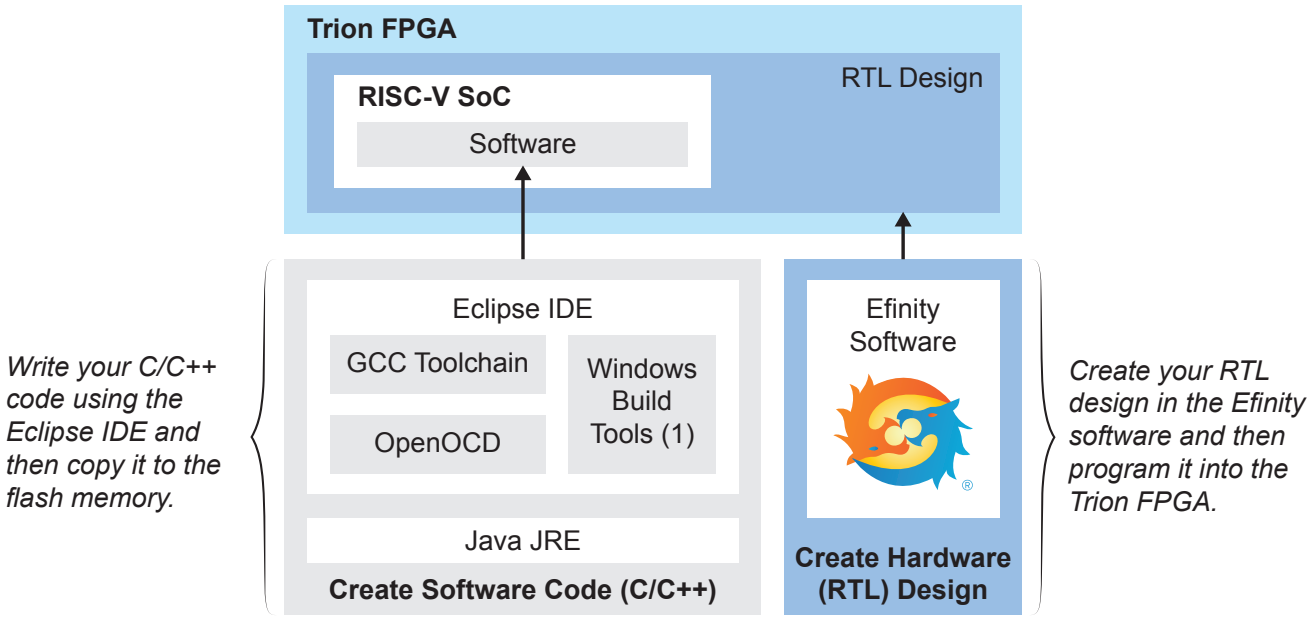


**Figure 2 SoC Design Flow**

## What's in the Package

With each RISC-V SoC, Efinix provides a complete package of hardware and software files. Additionally, to help you develop software applications, Efinix distributes a collection of pre-compiled open-source software.

### Hardware

- SoC RTL files
- SoC testbench
- Example design targeting an Efinix development board

### Software

- Board support package (BSP)
- Linker script
- SoC include header files
- OpenOCD configuration files
- Example software applications

### SDK

- Eclipse IDE for managing projects and software
- GCC compiler
- OpenOCD debugger for debugging
- Windows build tools (Windows)

## Efinity Software Support

The SoCs are fully supported by the Efinity© software, which provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, debugging, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The software-generated bitstream file configures Trion devices. The software supports the Verilog HDL and VHDL languages.

## Availability

All three RISC-V SoCs are available now for download from our Support Center www.efinixinc.com/support.





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