Reconfigurable Acceleration Platforms

Efinix® FPGAs have been widely adopted in a broad spectrum of applications from consumer electronics to edge compute, from AI image processing to industrial automation. They have a cost structure that can be used in high volume manufacturing, speeding time to market and eliminating financial and resource risks associated with designing custom ASICs. The FPGAs themselves are low power, making them a natural fit for demanding environmental conditions such as in surveillance or industrial automation applications.

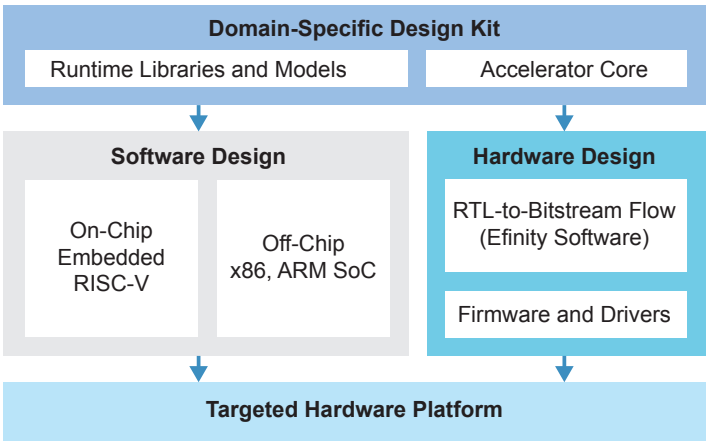
But sometimes a standalone FPGA is not enough. Efinix's Reconfigurable Acceleration Platform (RAP) is an initiative that helps designers intuitively incorporate FPGAs in applications in which they can provide domain-specific compute and acceleration and adapt to changing workloads over the life of the product. RAP provides:

- Hardware to balance time to market and costs for optimized solutions
- Software to deliver a natural abstraction of hardware to speed time to market
- Design flows to provide end-to-end support for mixed hardware/software systems

The RAP initiative lets you pick the technologies you need and assemble them in an easy-to-use package. You can start off using a standard off-the-shelf Trion or Trion Titanium FPGA. With chiplets, the first level of customization, you select components that best fit your application needs and combine them with an FPGA as a system-in-package (SIP).

The result is a custom solution with lower cost and faster time to market. The next level is monolithic integration, in which you embed a standard FPGA core into your own SoC. These solutions are best for high volumes. Finally, when you need a completely custom solution, Efinix can help you design a Quantum core to integrate into your ASIC. With RAP, you have a full range of solutions that can help you take your applications to the next level.

Complementing this enhanced hardware versatility, the RAP initiative also delivers an intuitive approach to system design and software partitioning. A standardized hardware accelerator interface lets you leverage the RISC-V cores available on Efinix FPGAs. You can build hardware accelerators in the FPGA, resulting in more intuitive hardware/software partitioning, reduced time to market, and dramatically improved system performance.



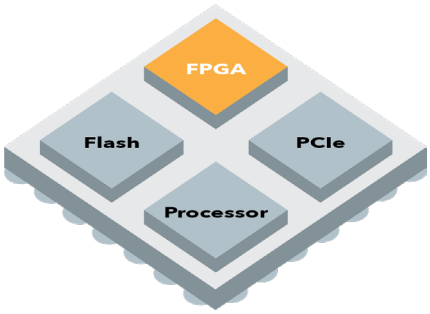
Harnessing FPGA potential to enhance versatility, reduce time-to-market, and minimize cost

Level 1: Standalone FPGAs

Trion® and Trion Titanium FPGAs

- Reconfigurable FPGA
- Embedded hardened IP
- Ready to use
- Efinity® Design Suite support
- Efinix soft IP ecosystem

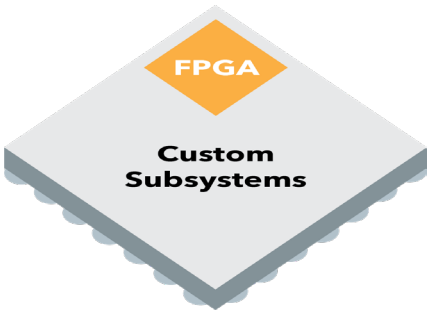
Level 2: Multi-Chip SIPs



Trion, Trion Titanium, and Subsystems Chiplets

- Known good die
- SIP packaging for minimal size
- Custom SIP configuration
- Efinity® Design Suite support
- Efinix soft IP ecosystem

Level 3: Domain Specific Silicon



Monolithic Integration of FPGA and Custom Subsystem

- Customer subsystems integrated with Trion or Trion Titanium framework
- Custom SoC configuration with Efinity® Design Suite support
- Efinix soft IP ecosystem

Level 4: Quantum™ Core Licensing

Monolithic Integration into Custom ASIC

- Quantum core in GDS
- Core integration guidelines
- Manufacturing test support
- Efinity® Design Suite support
- Efinix soft IP ecosystem

RAP-OVERVIEW-1.0

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