Trion® MIPI Interface PCB Design User Guide

UG-PCB-MIPI-v1.0
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Contents

Introduction

This user guide explains the recommended printed circuit board (PCB) layout design for the Trion® MIPI PHY signals. You should implement these best practices as well as understand your PCB layout options when designing MIPI applications.

You should place and route high-speed components and signals on the board first. Route high-speed clock and high-speed differential pairs first, and use the shortest trace lengths you can.

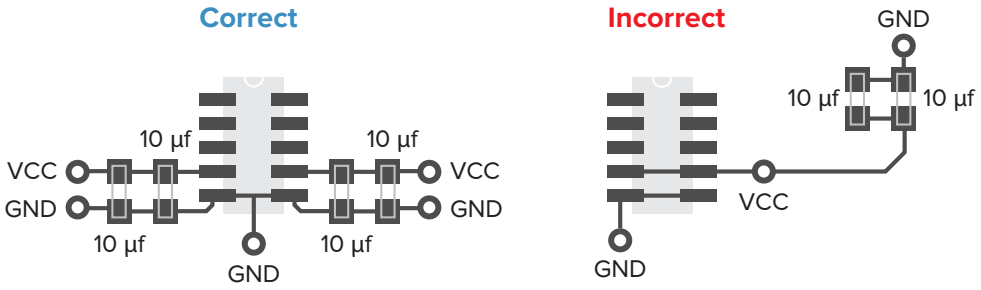
Placement Guidelines

The following sections describe guidelines for planing components on the board.

Placing Bypass Capacitors

Place bypass capacitors close to every integrated circuit's power supply pin.

Figure 1: Place Bypass Capacitors Close to IC Pins

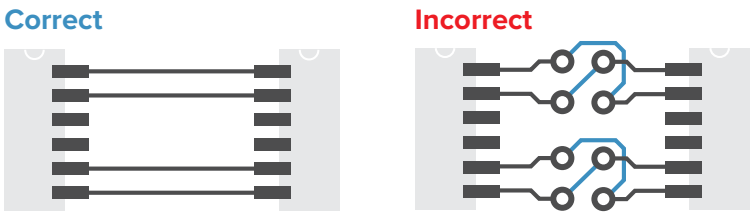


Placing Multi-Line Interfaces

When placing components, avoid crossing high-speed signals. The Trion® MIPI RX block supports polarity inversion, that is, you can swap the P and N pins for any MIPI physical lane. This feature eliminates the need to cross lanes.

Note: You set the polarity inversion in the Interface Designer using the **Swap P&N Pins** option.

Figure 2: Use Polarity Inversion when Possible



Differential Pair Signal Guidelines

For high-speed operation, you need to layout your PCB to improve signal quality at the receiver and reduce the loss of transmitted signals. By following signal routing best practices, you can minimize cross-talk between traces, reduce noise from the distributed power network, and switching noise during operation.

Match Trace Lengths

High-speed differential signals should be routed symmetrically. Always keep route signals in parallel with a constant distance between two traces. This distance is required to achieve the specified differential pair impedance. The following figures provide examples of correct and incorrect traces.

Figure 3: Route Differential Pairs Symmetrically and Always Keep Signals Parallel

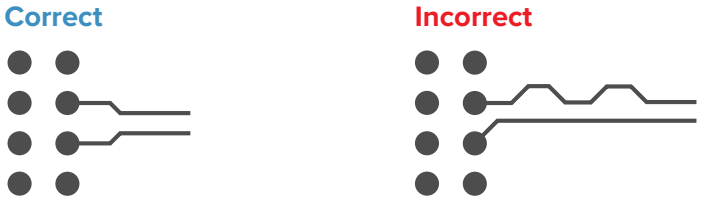


Figure 4: Do Not Place Components or Vias between Differential Pairs

Figure 5: Place Coupling Capacitors Symmetrically

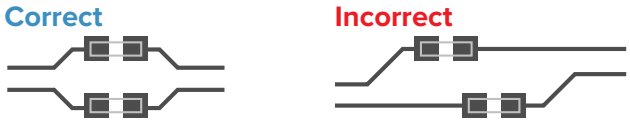


Figure 6: Place Vias Symmetrically

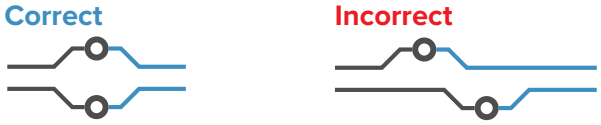
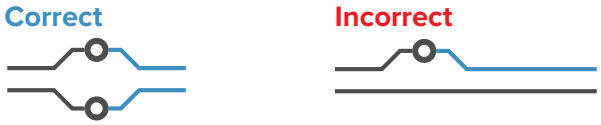
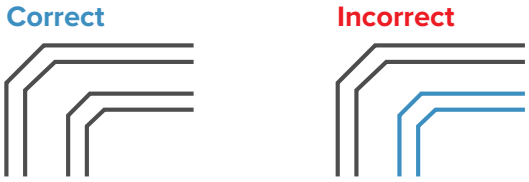


Figure 7: Route Pairs on the Same Layer with the Same Number of Vias



Signal speeds are different on different layers. For interfaces that require tight matching between signal pairs and the clock pair, route all the data and clock signals on the same layers.

Figure 8: Route Pairs from the Same Interface on the Same Layer



Add length correction near the mismatching point to ensures the differential pair signals are propagated synchronously over most of the connection.

Figure 9: Add Length Correction near the Mismatching Point

Isolate Noise

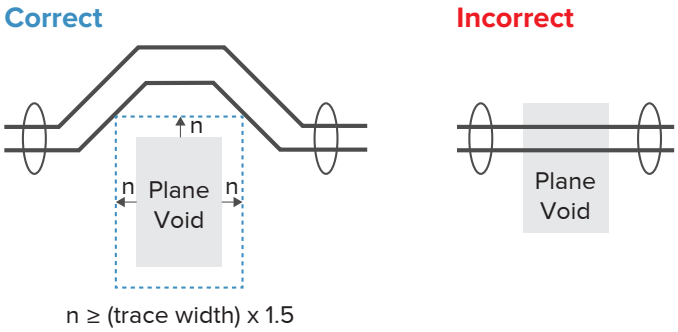
To limit the amount of signal noise, following these guidelines:

- Maintain the maximum possible distance between high-speed clocks and periodic signals going to high-speed differential pairs and any connector leaving the PCB (e.g., I/O connectors, control and signal headers, or power).
- To minimize crosstalk, keep the high-speed clock and periodic signal trace lengths that run parallel to high-speed signal lines as short as possible. Based on EMI testing, the minimum suggested spacing to clock signals is 50 mils.
- Keep high-speed signals clear of the core digital logic. Internal state transitions produce high-current transients, which can be very difficult to filter.

Avoid Routing in Reference Planes

Avoid routing high-speed signals in a reference plane. If it is absolutely necessary, route them over a solid GND reference plane and not across a split plane.

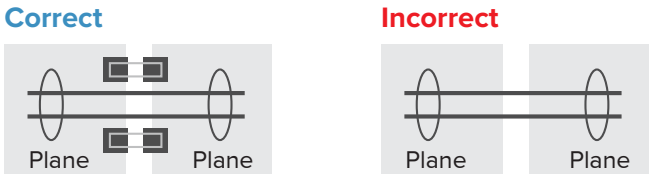
Figure 10: Avoid Route High-Speed Signals across a Split Plane



If you cannot avoid routing over a split plane, place stitching capacitors across the split to provide a return path for the high-frequency current. These stitching capacitors minimize the current loop area and any impedance discontinuity created by crossing the split.

- These capacitors should be 1 μF or lower.
- Place capacitors as close to the crossing planes as possible.

Figure 11: Use Stitching Capacitors across Split Planes



Controlling Impedance

An ideal transmission line has a characteristic impedance that matches the intended signal's transmitter and receiver. If the characteristic impedance of the matched transmission line is perfectly maintained, the receiver sees the transmitter's full signal at the end of the trace. There is no reflection or signal attenuation.

To control impedance, you need to control three features of the circuit's geometry:

- The trace width
- The spacing between the signal return path and the signal trace
- The dielectric coefficient of the material surrounding the trace

You can calculate these values using a trace impedance calculator. Work with your PCB manufacturer during your PCB layout design for these impedance calculations.

Additionally:

- Route high-speed signals using a minimum number of vias and corners to reduce signal reflections and impedance changes.
- To route a 90° turn, use two 45° turns or an arc instead of a single 90° turn. This method reduces reflections on the signal by minimizing impedance discontinuities.

The following table shows the typical high-speed trace impedance for the Trion® MIPI interface.

Table 1: MIPI Trace Impedance

Parameter	Min	Typ	Max	Units
MIPI D-PHY RX or TX differential impedance	90	100	110	Ω
MIPI D-PHY RX or TX single-ended impedance	45	50	55	Ω

Revision History

Table 2: Document Revision History

Date	Version	Description
May 2020	1.0	Initial release.