Titanium DDR DRAM PCB Design User Guide

UG-PCB-DDR-TI-v1.2
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Contents

Introduction

This user guide explains the recommended printed circuit board (PCB) layout design for the Titanium DDR DRAM interface signals. You must have basic knowledge of high-speed PCB layout design. You should implement these best practices as well as understand your PCB layout options when designing applications that incorporate DDR DRAM. Good signal integrity (SI) is important because poorly transmitted signals can significantly lower the data valid margin at the receiver.

Table 1: Titanium FPGA Pin Symbol and Description

Symbol	Titanium FPGA Pin Name		Description
	x16	x32	
DDR			LPDDR4 and LPDDR4x external memory interface
DRAM			External memory
VDD	VDD_PHY		LPDDR4 and LPDDR4x digital power supply
VDDQ	VDDQ_PHY		LPDDR4 and LPDDR4x I/O power supply
CA			Clock/control/command/address signals
SNR			Signal-to-noise ratio
Clock Signals			
CK	DDR_CK, DDR_CK_N		Differential clock
Command /Address Signals			
A	DDR_A[5:0]		Command/address bus
Control Signals			
CKE	DDR_CKE[1:0]		Clock enable
CS	DDR_CS_N[3:0]		Chip select
Data Signals			
DM	DDR_DM[1:0]	DDR_DM[3:0]	Data-mask signal enable
DQ	DDR_DQ[15:0]	DDR_DQ[31:0]	Data bus
DQS	DDR_DQS[1:0], DDR_DQS_N[1:0]	DDR_DQS[3:0], DDR_DQS_N[3:0]	Differential data strobe

In the document, the recommendation is based on FR4 material with a dielectric constant (D_k) value of 3.7 to 3.9 and a disspation factor (D_f) value of 0.012 to 0.02:

- Performance can vary depending on FR4 material, PCB stackup, trace impedance (Z_o), and layout implementation.
- The layout design must include the package net length for length matching.

Efinix® recommends that you perform SI analysis after completing the layout design.

General Guidelines

Efinix® recommends that you follow these general guidelines with respect to the length, skew, and impedance when laying out your board.

Power Design

- Route GND and VCC as planes.
- Place ground return vias within ±250 mils of transition vias.
- Keep reference plane continuous between FPGA and DRAM.
- Maintain isolation >-45 dB by keeping unrelated signals, power, and ground shapes away from DDR signal.

Decoupling Recommendations

- Use a high-accuracy capacitor to minimize inductance.
- Place every voltage supply decoupling capacitor close to pull-up resistors.
- For the VDD and VDDQ power supplies, use >0.1 µF decoupling capacitor to reduce noise.

Placement

- Place the DRAM device as near as possible to the Titanium FPGA.
- Rotate the IC orientation to have direct routing especially for high-speed traces.
- Avoid routing high-speed differential traces under power connectors, power delivery inductors, other interface connectors, crystal, oscillators, clock synthesizers, magnetic devices, or integrated circuits that use or duplicate clocks.
- Keep large spacing (> 100 mils) between high-speed traces, vias, and pads of high-noise power nets.

Note: High-noise power nets include nets like the switching node (phase node) of a voltage regulator module (VRM), 12 V power net, and high current transient power net.

Note: Refer to Titanium Interactive Hardware Design Checklist and Guidelines in Efinix® Support Center for further details.

Table 2: LPDDR PCB Stackup Example

PCB Layer	4 Layers	8 Layers	8 Layers	12 Layers
L1	DM/DQ/DQS/CA	CA	NA	CA
L2	Power/GND	GND	GND	GND
L3	Power/GND	DM/DQ/DQS	DM/DQ/DQS	DM/DQ/DQS
L4	DM/DQ/DQS/CA	Power/GND	Power/GND	GND
L5	-	Power/GND	Power/GND	Power
L6	-	DM/DQ/DQS	DM/DQ/DQS	Power
L7	-	GND	GND	GND
L8	-	NA	CA	DM/DQ/DQS
L9	-	-	-	GND
L10	-	-	-	DM/DQ/DQS
L11	-	-	-	GND
L12	-	-	-	NA

PCB Layout Design Recommendation

Table 3: PCB Layout Design Recommendation (From FPGA to DRAM Pin)

These numbers are the lengths calculated based on FR-4 material with Stripline (1 ps = ~5 mil). Please refer to **Table 4: Skew Control Recommendations** on page 12 for actual delay requirement.

PCB Trace Recommendation	Clock Signal	Command/ Address Signals	Control Signals		Data Signals			Unit
Signal	**CK**	**A**	**CKE**	**CS**	**DM**	**DQ**	**DQS**	
Impedance (±10%)	80	40	40	40	40	40	80	Ω
Blind via (Max)[1]	2	2	2	2	2	2	2	Qty
Width (Min)	5	5	5	5	5	5	5	mil
Spacing Between Trace								
Serpentine spacing to itself (Min)	15 (3x width)							mil
Spacing to DDR net (Min)	15 (3x width)							mil
Spacing to non-DDR net (Min)	25 (5x width)							mil
Spacing for byte_group to byte_group (Min)	-	-	-	-	25 (5x width) Keep the same byte group in same PCB layer.			mil
Spacing between differential pair	5 – 8	-	-	-	-	-	5 – 8	mil
Length Matching Tolerance								
Length difference between differential pair (Max)	5	-	-	-	-	-	10	mil
Length difference within same group (Max)	5	62.5	62.5	62.5	375	375	10	mil
Signal length minus CK length	-	±30	±30	±30	-	-	<0	mil
Signal length minus DQS length	>0	-	-	-	0 – 375	0 – 375	-	mil
Total Signal length for each signal (Max)	2.5	2.5	2.5	2.5	2.5	2.5	2.5	inch
Sequence to route	5	4	7	6	3	2	1	-

Important: Include the FPGA package net length when calculating length matching tolerance. See **Length Matching** on page 8.

[1] Refer to **Length Matching** on page 8 for the Blind via requirement.

Routing DDR Signals

- Minimize the PCB layer propagation variance.
- Avoid T-junctions for high-speed signals.
- Meet all delay matching requirements for PCB trace delays, different layer propagation velocity variances, and crosstalk.
- Surround the DRAM BGA pads with ground.
- To minimize the return path:
  - For the byte lanes, match all DQ and DQS traces by refering to **Table 3: PCB Layout Design Recommendation (From FPGA to DRAM Pin)** on page 6.
  - Route data groups next to a VSS plane.
- Avoid placing high-speed DQ, DQS, address, and control signal across split planes. See **Split Planes and Reference Planes** on page 11 for details.
- Use a gradual trace angle to reduce parasitic effects (avoid 90° trace angles). See **Bending Traces** on page 9 for details.

Clock Signals

The DDR DRAM interface requires different master DDR_CK and DDR_CK_N clock inputs. All address and control signals are sampled on the rising edge of DDR_CK.

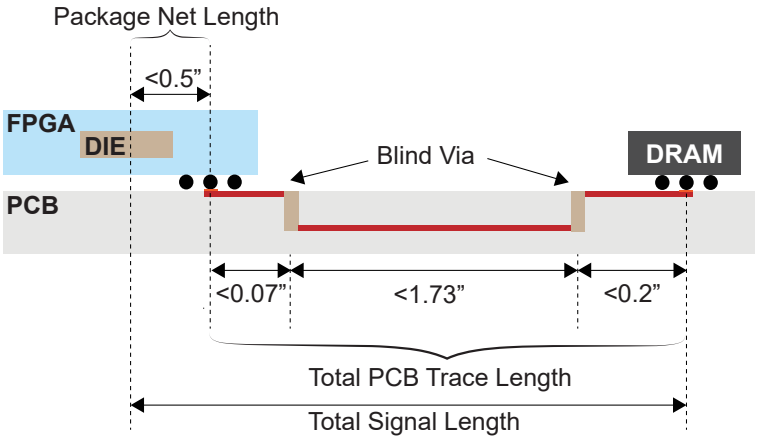
- Ensure that the DRAM has a clean differential clock input.
- Balance the output data so that each data word has the same valid time as all of the signals.
- Match the DDR_CK trace length to the DDR_CK_N trace length by referring to **Table 3: PCB Layout Design Recommendation (From FPGA to DRAM Pin)** on page 6. It is applicable for multiple clock pairs that are transmitted from the controller to components.
- Route all the CK, A, CKE, and CS in the same PCB layer.

Important: If you use the write leveling feature, the $CK_{(n-1)}$ trace length must be longer than the $DQS_{(n-1)}$ trace length. *n* is the number of DDR device used. Refer to **Table 4: Skew Control Recommendations** on page 12 for more skew control recommendations.

Length Matching

Efinix® recommends that you comply to the length matching tolerance in **Table 3: PCB Layout Design Recommendation (From FPGA to DRAM Pin)** on page 6. The length matching recommendation is derived from the total signal length. The following figure illustrates the total signal length.

Figure 1: Total Signal Length



The total signal length is (FPGA package net length + total PCB trace length). You can obtain the FPGA package net length file from **Package Net Length** in Efinix®Support Center.

The distance requirement of the PCB trace length involving the Blind vias is as follows:

- Maximum distance between FPGA ball and Blind via – 70 mils.
- Maximum distance between DRAM ball and Blind via – 200 mils.

For example, if the package delays for the three pins reported in the FPGA package net length file are:

- Pin A1—110 ps
- Pin A2—70 ps
- Pin A3—150 ps

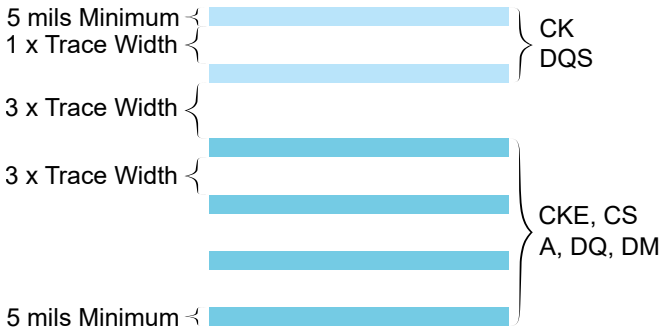
To match the total signal length of 3 pins, you would need to have a PCB trace for Pin A1 that is 40 ps longer than Pin A3 and a PCB trace for Pin A2 that is 80 ps longer than Pin A3.

Trace Spacing

When planning your board's signal traces, maintain the correct spacing between traces. The minimum trace width for all DDR signals is 5 mils.

- 3H spacing between any data and address/command traces, where H is the distance to the nearest return path.
- 5H spacing between memory clock and any other signals, where H is the distance to the nearest return path.

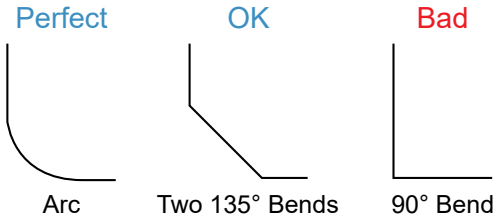
Figure 2: Trace Spacing Guidelines



Bending Traces

Avoid bending high-speed signal traces. When bending is required, use a bend angle greater than 135° to ensure that the bend is as loose as possible.

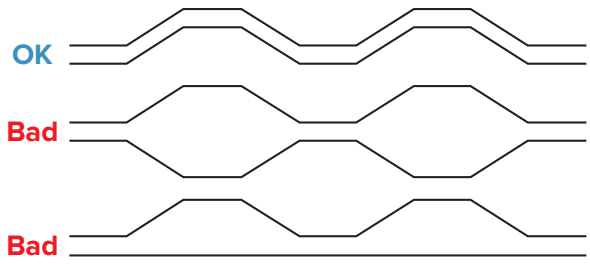
Figure 3: Examples of Trace Bends



Differential Pair Symmetry

Route all high-speed differential pairs together symmetrically and parallel to each other.

Figure 4: Pair Symmetry Examples



Match Trace Lengths

High-speed differential signals should be routed symmetrically. Always keep route signals in parallel with a constant distance between two traces. This distance is required to achieve the specified differential pair impedance. The following figures provide examples of correct and incorrect traces. The different trace colours indicate different PCB layers.

Figure 5: Route Differential Pairs Symmetrically and Always Keep Signals Parallel

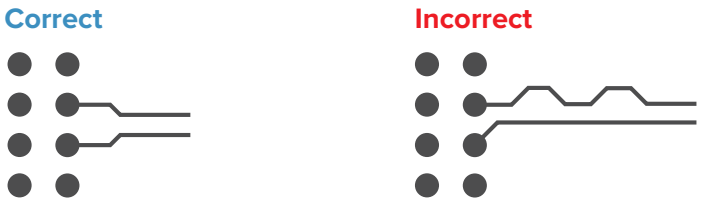


Figure 6: Do Not Place Components or Vias between Differential Pairs

Figure 7: Place Vias Symmetrically

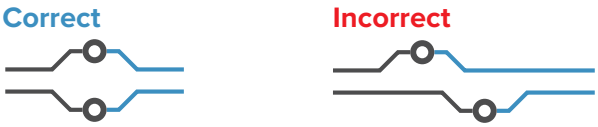
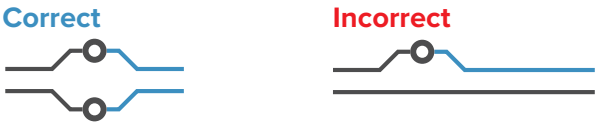
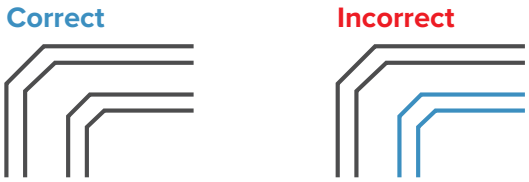


Figure 8: Route Pairs on the Same Layer with the Same Number of Vias



Signal speeds are different on different layers. For interfaces that require tight matching between signal pairs and the clock pair, route all the data and clock signals on the same layers.

Figure 9: Route Pairs from the Same Interface on the Same Layer



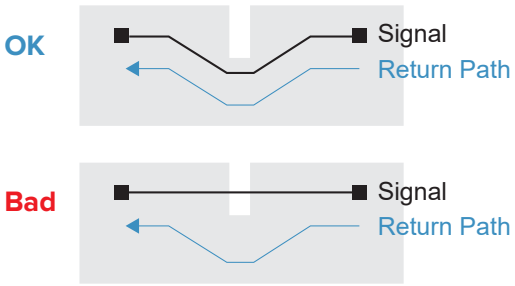
Add length correction near the mismatching point to ensure the differential pair signals are propagated synchronously over most of the connections.

Figure 10: Add Length Correction near the Mismatching Point

Split Planes and Reference Planes

High-speed signals should be routed over a ground plane. Do not route these traces across a split plane or reference plane, even when using microstrip or stripline methods. Routing across a plane split or a void in the reference plane forces the returned high-frequency current to flow around the split. The reflection increases impedance and the signal delay is increased by series inductance.

Figure 11: Split Plane Examples



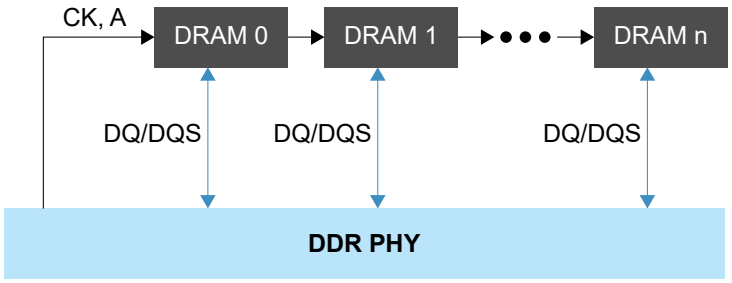
Fly-By Layout For Multiple DRAM Devices

If you plan to use two or more DRAM devices on your board, Efinix® recommends using a fly-by layout. This method:

- Avoids T-junctions on the PCB thereby improving the SNR.
- Reduces the trace lengths between the devices.
- $CK_{(n-1)}$ trace length must be longer than the $DQS_{(n-1)}$ trace length. *n* is the number of DDR device used.

If you are only using one DRAM device, a fly-by design is not applicable.

Figure 12: Fly-By Example Layouts

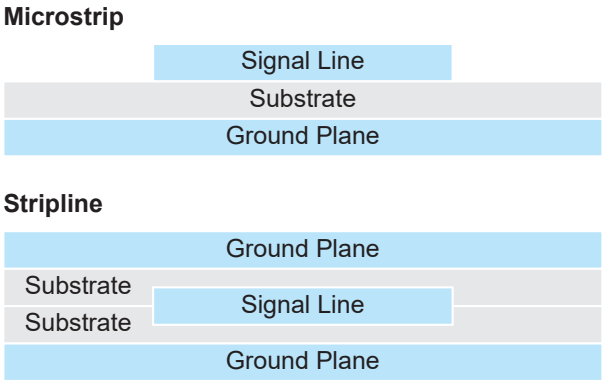


Controlling Skew

Microstrip and Stripline Skew

Two common methods to route high-speed lines are stripline, which sandwiches the signal line between ground planes, and microstrip, which lays the signal line on the board's surface. Efinix® recommends using stripline because it provides a better SNR for high-speed signals and helps to reduce skew.

Figure 13: Comparing Microstrip and Stripline Design



Skew is the timing delay difference between 2 or more signals. The following table shows skew control recommendations for double data rate and single data rate domains for various operating frequencies, as well as the recommended PCB skew for CK to DQS timing.

Note: The timing information provided here is for reference only. The layout, PCB, and components you use will affect the actual signal timing and skew.

Table 4: Skew Control Recommendations

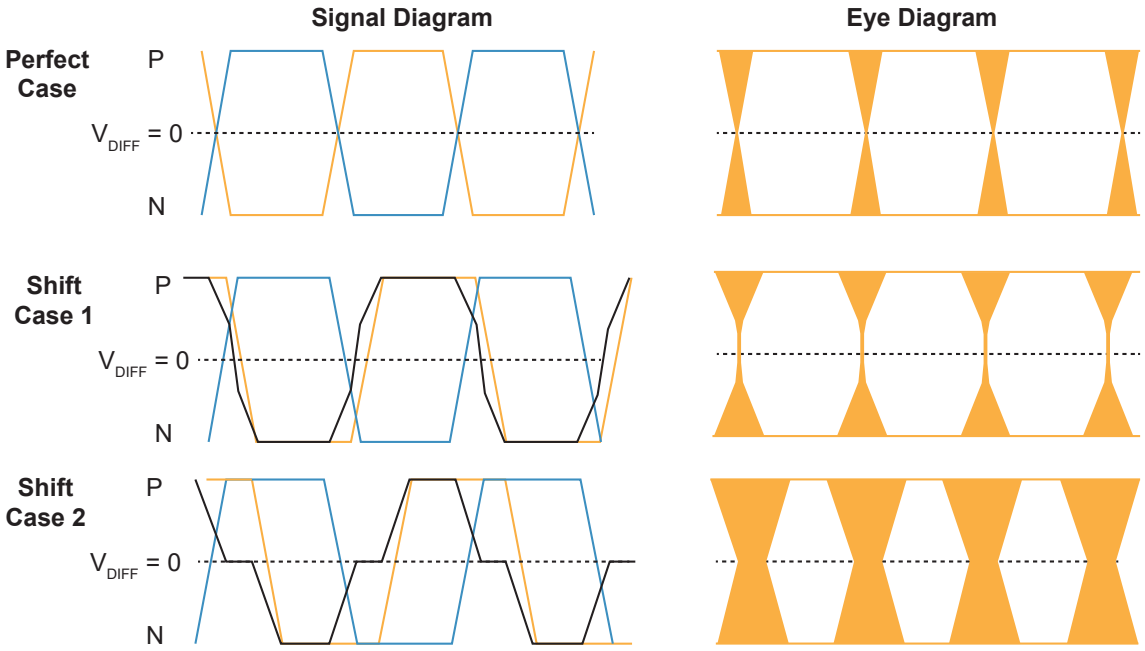
Speed (Bit Rate)		3700 Mbps LPDDR4	3700 Mbps LPDDR4x	Unit
DQ to DQS	Max Skew	75	75	ps
CK to DQS	Max Skew	350	350	ps
A, CKE, CE to CK	Max Skew	100	100	ps

Differential Pair Skew

For correct DRAM operation, the timing of the DQS and CK differential pairs is critical. Efinix® strongly recommends that you match the electrical length between these legs and keep any differences to less than 1 ps.

Skew between the differential pair lines (intra-pair skew) impacts the monotonicity of the CK and DQS signals, which are critical to the timing. Skew on these signals causes signal distortion and increases the bit error rate.

Figure 14: Effect of Intra-Pair Skew on Eye Diagram



Note: The Titanium DDR DRAM controller cannot deskew the differential signals. The zero crossing of the differential signals can seriously impact timing margins, leading to high jitter, high SNR, and increased sample errors.

Table 5: Trace Length's Effect on Signal Integrity

Property	Pin Match	Pin Mismatch
Length	< ±1% of trace length	> ±1% of trace length
Skew	< ±1 ps	> ±1 ps
Delay	No skew	Skew
Jitter	Low	High
Sample error	Low	High
SNR	Low	High
Distortion	Low	High

Controlling Impedance

An ideal transmission line has a characteristic impedance along the entire trace. If the characteristic impedance of the matched transmission line is perfectly maintained, the full signal exists at the end of the trace without reflection or signal attenuation.

To control impedance, you need to control three features of the circuit's geometry:

- The trace width.
- The spacing between the signal return path and the signal trace.
- The dielectric coefficient of the material surrounding the trace.

You can calculate these values using a trace impedance calculator. Work with your PCB manufacturer during your PCB layout design for these impedance calculations.

Additionally:

- Use 40 ±10% for all single-ended signals.
- Use 80 Ω ±10% for all differential signals.
- Route high-speed signals using a minimum number of vias and corners to reduce signal reflections and impedance changes.
- To route a 90° turn, use two 135° turns or an arc instead of a single 90° turn. This method reduces reflections on the signal by minimizing impedance discontinuities.

Revision History

Table 6: Document Revision History

Date	Version	Description
December 2022	1.2	Removed Titanium FPGAs with a Hardened DRAM Interface and DDR Comparison topics. Updated Skew Control Recommendation table.
October 2022	1.1	Updated Blind vias in table: **Table 3: PCB Layout Design Recommendation (From FPGA to DRAM Pin)** on page 6 and **Length Matching** on page 8. (DOC-926) Updated table: Titanium DDR Features. Updated table: **Table 2: LPDDR PCB Stackup Example** on page 5 Updated table: **Table 4: Skew Control Recommendations** on page 12
September 2022	1.0	Initial release.