AN 057: Controlling VQPS with the Efinity® SVF Player

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Introduction

Titanium FPGAs have a bitstream security feature that prevents tampering with the FPGA and protects your intellectual property. You use tools provided with the Efinity®software to turn on bitstream encryption or authentication, generate keys, blow security fuses, and sign bitstreams.

Your security settings are permanently stored in the FPGA in fuses. After these fuses are blown, you cannot change the settings. To ensure that the fuses are blown only when intended, Titanium FPGAs have a dedicated power supply pin (VQPS). You follow a specific power sequence for this pin when blowing the fuses.

This document describes how to power up VQPS automatically using a FTDI mini-module (FTDI n232H chipset), the Efinity SVF Player, and an on-board circuit to blow Titanium fuses.

Note: Refer to the data sheet or pinout to determine whether your Titanium FPGA has a VQPS pin.

The general procedure is:

- Design your board to include a circuit to control the VQPS pin's power.
- Include a header to connect the JTAG mini-module to the enable pin of the VQPS power circuit (you can use a 2-pin header or an available pin from the existing JTAG header).
- Set an environment variable.

Note: This document assumes that you are familiar with the Titanium fuse programming requirements and with the Efinity tools you use for bitstream security. For more information on these topics refer to:

"Security Feature" in the Titanium data sheet.

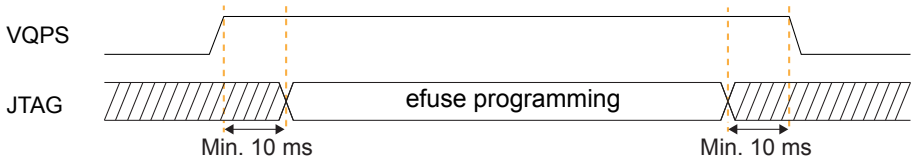
"Securing Titanium Bitstreams" in the **Efinity Software User Guide**.

VQPS Power Guidelines

Follow these guidelines for your circuit board:

- Your board must connect the VQPS pin to ground *before* powering up the FPGA and *after* fuse programming.
- During fuse programming, power the VQPS pin with 1.8 V using an on-board circuit or via an external power supply.
- Use one signal from the FTDI mini-module to turn on power to the VQPS pin so you can easily control it with the mini-module and the Efinity SVF Player.

Figure 1: Fuse Programming Waveform

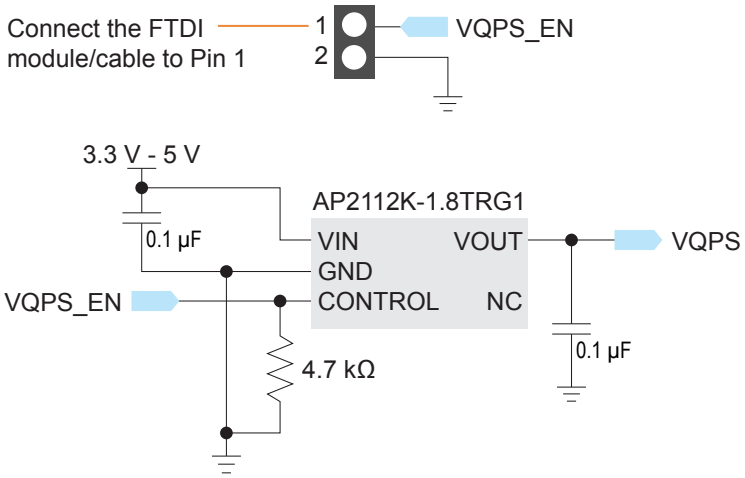


VQPS Circuit

Your circuit board should include an external circuit to control the VQPS power supply (e.g., an LDO linear voltage regulator or relay). This circuit should have:

- A fixed 1.8 V output voltage.
- An output current of 100 mA minimum.
- A method to turn the power to the VQPS pin on or off.
- An automatic discharge when disabled or turned off.

Figure 2: Example VQPS Circuit

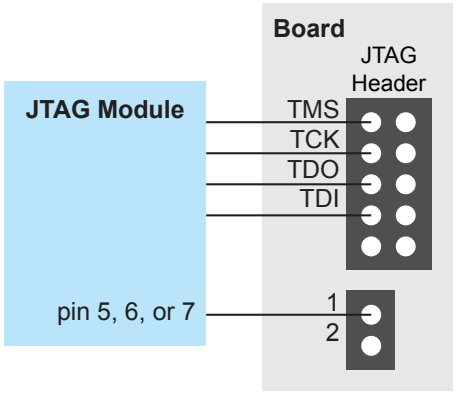


This example circuit uses the AP2112K-1.8TRG1 LDO linear voltage regulator from Diodes Incorporated.

JTAG Mini-Module Connection

The following figure shows a conceptual diagram of how your board connects to the JTAG mini-module.

Figure 3: Connection between Board and JTAG Mini-Module



You connect the JTAG signals as usual. You connect pin 4, 5, 6, or 7 to the 2-pin header that connects to the `VQPS_EN` pin. You can use any channel on the mini-module. Note the channel and pin number; you use them to set an environment variable for the SVF Player.

Efinity Environment Variable

You use an environment variable to tell the Efinity SVF Player which min-module pin is controlling the `VQPS_EN` signal. You add the variable to your environment using the `set` command (Windows) or `export` command (Linux) in a command window or terminal. The variable format is:

Windows: `set` *m*`BUS`*n*`_HIGH_DURING_TEST = 1`

Linux: `export` *m*`BUS`*n*`_HIGH_DURING_TEST = 1`

where:

- *m* is the FTDI mini-module channel (e.g., `BD`).
- *n* is pin `5`, `6`, or `7`.

Windows example:

```
set SET_BDBUS5_HIGH_DURING_TEST = 1
```

Linux example:

```
export SET_BDBUS5_HIGH_DURING_TEST = 1
```

Note: Ensure that the SVF Player recognizes the JTAG mini-module before powering up the FPGA.

The SVF Player controls the powering up and down of `VQPS`.

Methodology

The following steps describe the methodology:

1. Set up the environment variable for the pin that connects to the `VQPS` circuit.
2. With power to your board turned off, connect the FTDI mini-module to the headers that connect to the FPGA and `VQPS` circuit.
3. Open the Efinity SVF Player.
4. Ensure that the SVF Player can connect to the FTDI mini-module by clicking the Refresh USB Target button.
5. Power up the FPGA and `VQPS` circuit.
6. Use the SVF Player to run the **.svf** file.

Revision History

Table 1: Document Revision History

Date	Version	Description
March 2024	1.0	Initial release.