



# AN 036: Using the Standby Mode Feature

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# Introduction

Trion® FPGAs are manufactured on a low-power process and use a 1.1 V or 1.2 V core power supply during normal operation. To reduce the power consumption even further, these FPGAs support a standby mode in which you can power the FPGA down to 0.8 V and then wake it up to resume normal operation at 1.1 or 1.2 V. During standby mode, the FPGA retains its configuration so that it can resume operation immediately upon waking without taking the time to reconfigure. This feature is useful for applications that need to preserve battery power or require very low power consumption.

This application note describes how to trigger the Trion® FPGA to enter standby mode and exit it. Additionally, it provides the power consumption you can expect while in standby mode.

## Entering Standby Mode

To place the Trion® FPGA into standby mode, perform these actions in sequence:

1. Assert the reset signals for the PLL (RSTN). For FPGAs with MIPI CSI-2 and/or DDR DRAM hard blocks, assert the reset signals for the MIPI CSI-2 RX and TX (DPHY\_RSTN and RSTN), and DDR controller (CFG\_RST\_N). These signals should remain asserted while the FPGA is in standby mode.
2. Disable the clock tree. Efinix recommends instantiating a EFX\_GBUFCE primitive for each clock signal and using it to control the clocks. See [Controlling Clocks with the EFX\\_GBUFCE Primitive](#) on page 4 for details.  
Alternatively, you can disable the clock source externally.
3. Float the VCCIO\_DDR voltage (for FPGAs with hardened DDR interfaces).
4. Reduce the core power supply (VCC) to 0.8 V.



**Note:** Do not change the VCCIO voltages.

While the FPGA is in standby mode, minimal input transitions are required.

# Exiting Standby Mode

To wake the Trion® FPGA from standby mode, perform these actions in sequence:

1. Increase the core power supply (VCC) from 0.8 V to 1.1 V or 1.2 V using the correct power supply ramp rate.

**Table 1: Power Supply Ramp Rates**

Symbol	Description	Min	Max	Units
$t_{RAMP}$	Power supply ramp rate for all supplies.	0.01	10	V/ms

2. Power on the VCCIO\_DDR (for FPGAs with hardened DDR interfaces).
3. Turn on the clock tree. See [Controlling Clocks with the EFX\\_GBUFCE Primitive](#) on page 4.
4. Release the reset signals for the PLL (RSTN)  
For FPGAs with MIPI CSI-2 and/or hardened DDR interfaces, release the reset signals for the MIPI CSI-2 RX and TX (DPHY\_RSTN and RSTN) and DDR controller (CFG\_RST\_N).
5. Perform a system reset.

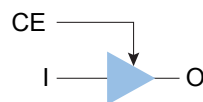
## Controlling Clocks with the EFX\_GBUFCE Primitive

To use the Trion® standby mode feature, you need to instantiate EFX\_GBUFCE primitives on every clock input. To turn off a given clock, drive the CE port low. To turn the clock back on, drive the CE port high.

The EFX\_GBUFCE logic block represents the global clock buffer driving the global clock network. The CE port gates the clock and is active high.

You must connect all EFX\_GBUFCE input ports. If you do not use a port, connect it to ground or V<sub>CC</sub> depending on its polarity. The software issues an error if the clock input I is set to V<sub>CC</sub> or ground.

**Figure 1: EFX\_GBUFCE Symbol**



**Table 2: EFX\_GBUFCE Ports**

Port Name	Direction	Description
I	Input	Input data
CE	Input	Clock enable
O	Output	Output data

The function table assumes all inputs are active-high polarity.

**Table 3: EFX\_GBUFCE Function**

Inputs		Output
CE	I	O
0	X	0
1	0	0
1	1	1

**Figure 2: EFX\_GBUFCE Verilog HDL Instantiation**

```

EFX_GBUFCE # (
    _CE_POLARITY(1'b1)    // 0 active low, 1 active high
) EFX_GBUFCE_inst (
    .O(O),                // Clock output to global clock network
    .I(I),                // Clock input
    .CE(CE)               // Clock gate
);

```

**Figure 3: EFX\_GBUFCE VHDL Instantiation**

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library efxphysicallib;
use efxphysicallib.efxcomponents.all;

entity gbufce_i_VHDL is
    port
    (
        clk, d, ce : in std_logic;
        q : out std_logic
    );
end gbufce_i_VHDL;

architecture behavioral of gbufce_i_VHDL is
    signal clknet : std_logic;
begin

    dut : EFX_GBUFCE
        port map (
            CE => ce,
            I  => clk,
            O  => clknet
        );

    ffx : EFX_FF
        port map (
            Q => q,
            D => d,
            CLK => clknet,
            CE => '1',
            SR => '0'
        );

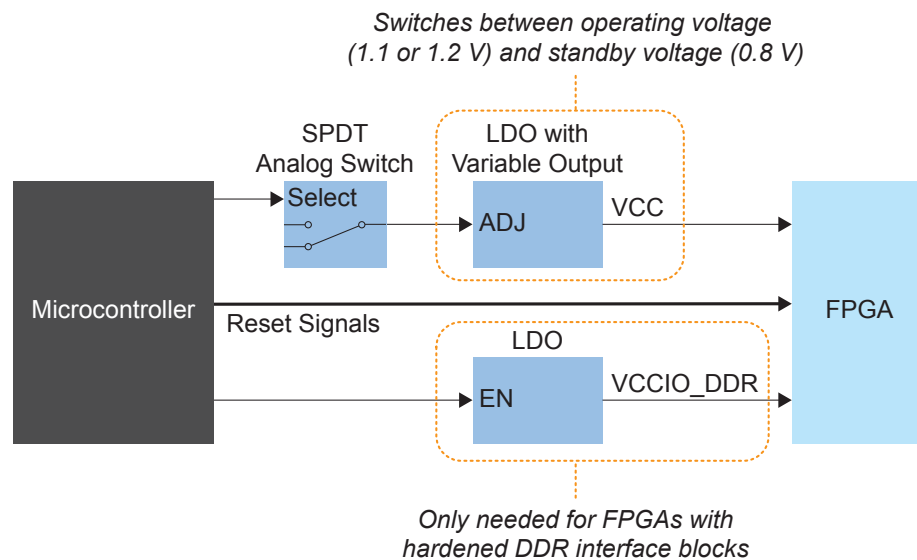
end behavioral;

```

# Standby Mode System Example

The following diagram shows an example system using a microcontroller, two low dropout voltage regulators (LDO), and a single pole double throw (SPDT) analog switch to use the standby mode feature. The microcontroller puts the FPGA into standby mode and wakes it up using the steps described previously.

**Figure 4: Example Microcontroller System for Standby Mode**



The microcontroller controls the FPGAs reset signals (for the PLL, MIPI CSI-2, and DDR controller), the LDO for the VCCIO\_DDR, and the SPDT switch. The microcontroller can also control the clock tree, or you can use another method to enable/disable the FPGA's external clock sources.

The variable output LDO supplies the VCC power to the FPGA at the operating voltage of 1.1 or 1.2 V or the standby voltage of 0.8 V, depending on the setting coming from the SPDT analog switch. You only need the LDO to enable or disable the VCCIO\_DDR power for FPGAs that have hardened DDR interface blocks.

# Expected Power Consumption

Efinix tested the power used in standby mode after following the recommended sequence. The following table summarizes the results.

*Table 4: FPGAs Tested in Standby Mode*

FPGA	Standby Power
T120 F324	20 mW
T20 F256	400 $\mu$ W



**Note:** For the T120, if you do not float the VCCIO\_DDR voltage, the system drives an additional current of 15 mA (12 mW) for VCC and 9 mA (10.8 mW) for VCCIO\_DDR, resulting in a total additional power consumption of about 23 mW. Therefore, for the lowest power consumption in standby mode for T120 FPGAs, Efinix recommends floating VCCIO\_DDR.

## Revision History

*Table 5: Revision History*

Date	Version	Description
June 2021	1.0	Initial release.