AN 028: Using the Memory Efficiency Tester

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Contents

Introduction

Efinix® provides a memory efficiency tester that you can use to test your DDR DRAM and HyperRAM memory performance. The memory efficiency tester includes the following features:

- Memory bandwidth calculation
- User-defined test options:
  - Read and write pattern combinations
  - Running address
  - Loop and burst length
- Pseudo-random read and write and comparison with a 128-bit linear-feedback shift register (LFSR)
- Total running-time cycle counter
- 256-bit AXI bus on AXI0
- Includes an example design targeting the Trion® T120 BGA324 Development Board and Titanium Ti60 F225 Development Board

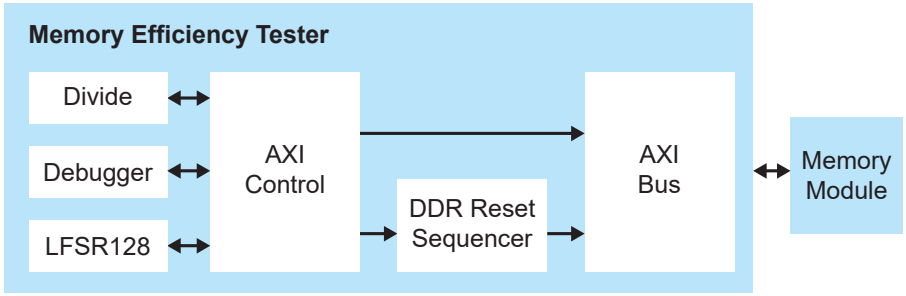
FPGA Support

The memory efficiency tester supports all Trion® with DDR DRAM and Titanium FPGAs with HyperRAM.

Functional Description

The memory efficiency tester is a utility design that you program into your board. You use the Efinity® Debugger to access the memory efficiency tester design parameters and obtain the performance test results.

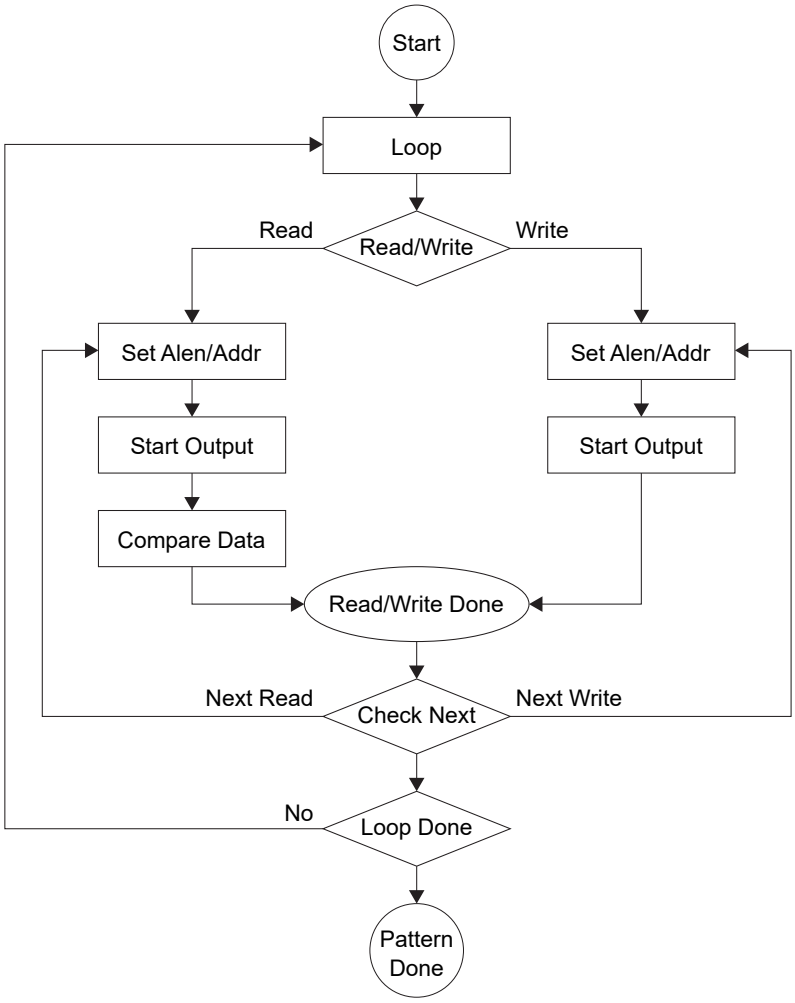
Figure 1: Memory Efficiency Tester Block Diagram



The memory efficiency tester consists of the following blocks:

- *DIVIDE*—Divider that performs division to calculate the bandwidth.
- *LFSR128*—Linear feedback shift register for write or read random data.
- *Debugger*—Connects with the tester to the Efinity® Debugger user interface.
- *AXI control*—Controls the pattern flow to output or input.
- *DDR reset Sequencer*—DDR controller reset block. (Not applicable in Titanium Ti60 F225 Development Board design)
- *AXI BUS*—Interface between the memory efficiency tester with the memory.

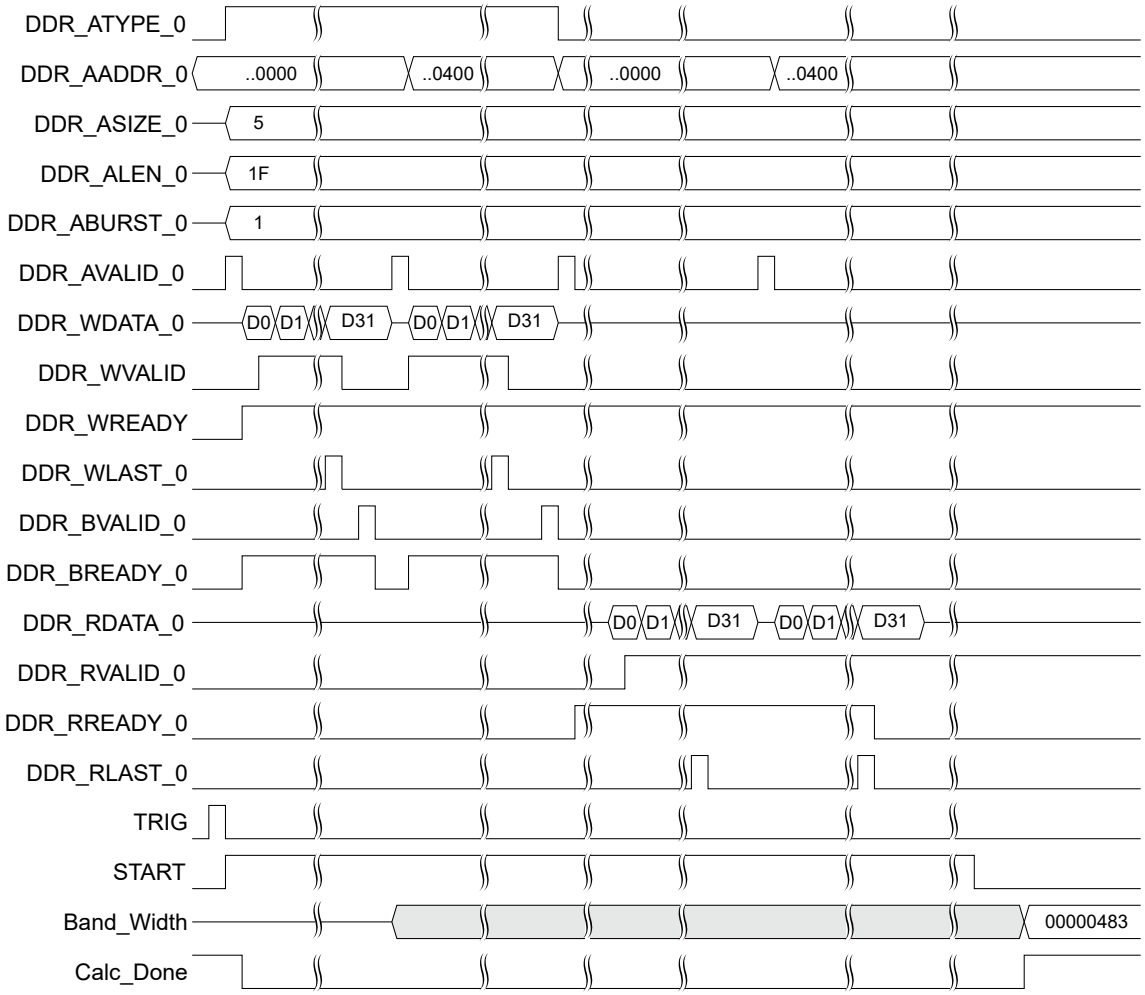
Figure 2: Memory Efficiency Tester Flow Diagram



Memory Efficiency Tester Waveform

The following waveform example shows the memory efficiency tester signals. The memory efficiency tester starts when the `TRIG` signal toggles high and low. The test ends when the `START` signal goes low. The memory bandwidth results calculation completes when the `Calc_Done` signal goes high.

Figure 3: Memory Efficiency Tester Waveform Example (Trion)



Virtual I/O Debug Core Sources and Probes

The memory efficiency tester includes a Virtual I/O debug core with the following sources and probes.

Table 1: Virtual I/O Debug Core Sources and Probes

Name	Type	Width	Description
LOOP_N	Source	32	Number of pattern loops. 0 = One loop only (default)
PATTERN	Source	16	0: Read 1:Write Default = 0x3333 This pattern together with PATTERN_DEPTH = 0xF, yields the following test pattern: W>W>R>R>W>W>R>R>W>W>R>R>W>W>R>R
PATTERN_DEPTH	Source	4	Selected pattern from 0 to 15. Default: 0xF (15)
PATTERN_LEN0	Source	8	First read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN1	Source	8	Second read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN2	Source	8	Third read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN3	Source	8	Fourth read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN4	Source	8	Fifth read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN5	Source	8	Sixth read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN6	Source	8	Seventh read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN7	Source	8	Eighth read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN8	Source	8	Ninth read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN9	Source	8	Tenth read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN10	Source	8	Eleventh read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN11	Source	8	Twelve read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN12	Source	8	Thirteenth read/write ALEN of AXI. Default: 0x1F

Name	Type	Width	Description
PATTERN_LEN13	Source	8	Fourteenth read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN14	Source	8	Fifteenth read/write ALEN of AXI. Default: 0x1F
PATTERN_LEN15	Source	8	Sixteenth read/write ALEN of AXI. Default: 0x1F
PATTERN_ADDR0	Source	32	First read/write address of AXI. Default: 0x0000 The next address must be PATTERN_LEN0 x 256 / 8.
PATTERN_ADDR1	Source	32	Second read/write address of AXI. Default: 0x0400
PATTERN_ADDR2	Source	32	Third read/write address of AXI. Default: 0x0000
PATTERN_ADDR3	Source	32	Fourth read/write address of AXI. Default: 0x0400
PATTERN_ADDR4	Source	32	Fifth read/write address of AXI. Default: 0x0000
PATTERN_ADDR5	Source	32	Sixth read/write address of AXI. Default: 0x0400
PATTERN_ADDR6	Source	32	Seventh read/write address of AXI. Default: 0x0000
PATTERN_ADDR7	Source	32	Eighth read/write address of AXI. Default: 0x0400
PATTERN_ADDR8	Source	32	Ninth read/write address of AXI. Default: 0x0000
PATTERN_ADDR9	Source	32	Tenth read/write address of AXI. Default: 0x0400
PATTERN_ADDR10	Source	32	Eleventh read/write address of AXI. Default: 0x0000
PATTERN_ADDR11	Source	32	Twelve read/write address of AXI. Default: 0x0400
PATTERN_ADDR12	Source	32	Thirteenth read/write address of AXI. Default: 0x0000
PATTERN_ADDR13	Source	32	Fourteenth read/write address of AXI. Default: 0x0400
PATTERN_ADDR14	Source	32	Fifteenth read/write address of AXI. Default: 0x0000
PATTERN_ADDR15	Source	32	Sixteenth read/write address of AXI. Default: 0x0400
Reset	Source	1	Resets or starts the memory tester. 0: Reset (default) 1: Normal

Name	Type	Width	Description
Pause	Source	1	Pauses the memory tester. 0: Normal (default) 1: Pause
Total_ALEN	Probe	64	Calculates total burst.
Cycle_Counter	Probe	64	Total cycles used.
Test_Done	Probe	1	Indicates the test status. 0: Busy 1: Done
Band_Width_MBs	Probe	32	Displays the calculated bandwidth in MB/s after test is done.
ERROR	Probe	1	Flags if an error occurred after comparing read data. 0: No error 1: Error

Memory Efficiency Tester Example Design

The memory efficiency tester includes an example design for the Trion® T120 BGA324 Development Board and Titanium Ti60 F225 Development Board that calculates the memory bandwidth. You can define the write and read pattern sequence to test the performance of the memory bandwidth.

Table 2: Trion® T120 BGA324 Development Board Example Design Implementation

FPGA	LUTs	Memory Blocks	f_{MAX} (MHz)	Language	Efinity® Version
T120 BGA324 C4	11,479	502	109.629	Verilog HDL	2021.2

Table 3: Titanium Ti60 F225 Development Board Example Design Implementation

FPGA	eXchangeable Logic and Routing (XLR) Cells	Memory Blocks	f_{MAX} (MHz)	Language	Efinity® Version
Ti60 F225 C4	12,945	245	198.242	Verilog HDL	2021.2

Download the Memory Efficiency Tester Example Design to the Board

The memory efficiency tester includes a bitstream file to get you started quickly. Download it to the board using these steps:

1. Download the file **efx_memory_tester-v<version>.zip** from the Support Center.
2. Open the project (**memory_tester.xml**) in the Efinity software. The project is located in the **efx_memory_tester-v<version>/<devboard>_dk** directory.
3. Review the design.
4. Connect the development board to your computer using a USB cable.
5. Use the Efinity® Programmer to download the bitstream file, **memory_tester.hex**, to your board. The bitstream file is in the **efx_memory_tester-v<version>/<devboard>_dk** directory.

   The boards's CDONE LED, D6 (Trion® T120 BGA324 Development Board) and D15 (Titanium Ti60 F225 Development Board) turns on when configuration completes.

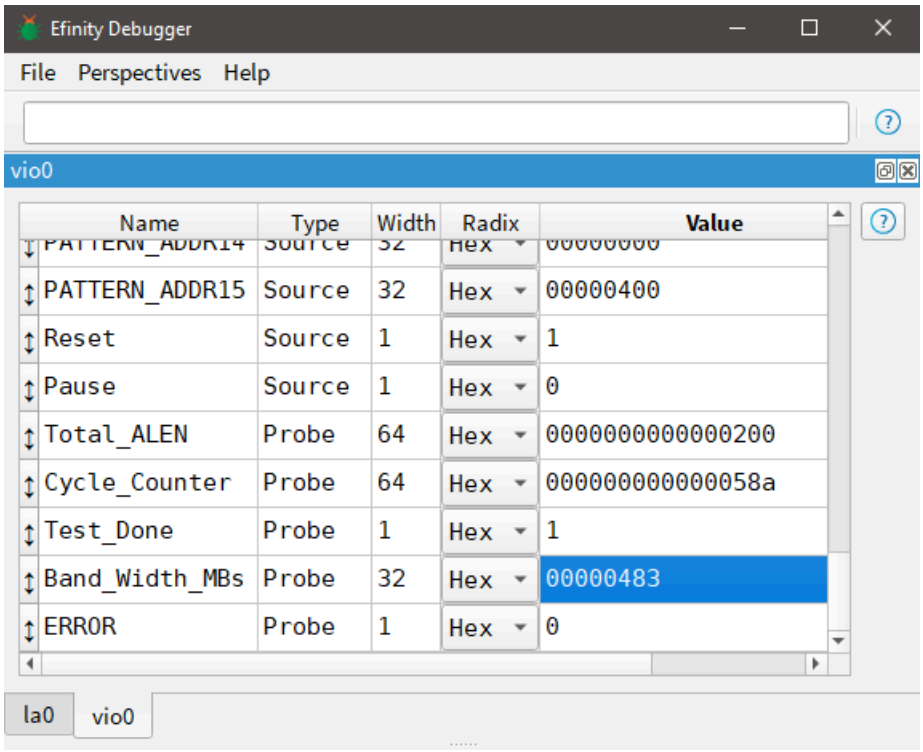
Learn more: Instructions on how to use the Efinity® software and board documentation **are available in the Support Center**.

Using the Memory Efficiency Tester

The following instructions assume that you have already programmed your board with the memory efficiency tester bitstream. To use the memory efficiency tester in the Debugger:

1. Open the Debugger. The tool opens to the Debug perspective.
2. If not already selected, select your board in the USB Target pull-down menu.
3. Click the Connect Debugger button.
4. The `VIO_0` debug core sources and probes displays.
5. Change the `Reset` to 1 and the tester starts calculating the memory bandwidth. The `Test_Done` value turns 0 to indicate the memory tester is calculating the memory bandwidth.
6. The `Test_Done` value changes to 1 when calculation completes and the `Band_Width_MBs` displays the memory bandwidth.

Figure 4: Example of Memory Efficiency Tester in Debugger



Important: The example design uses the Trion® T120 BGA324 Development Board and Titanium Ti60 F225 Development Board. You can incorporate the memory efficiency tester in your own design to test the memory performance on your own board. However, you may need to change the memory and PLL block settings in the Efinity® Interface Designer to match what you have on your board.

Revision History

Table 4: Document Revision History

Date	Version	Description
September 2022	1.3	Updated typo in Table 1 and Figure 2. (DOC-893)
April 2022	1.2	Updated Trion® T120 BGA324 Development Board design implementation with Efinity software v2021.2.
April 2022	1.1	Added support for Titanium FPGAs and design example for Titanium Ti60 F225 Development Board. (DOC-776)
November 2020	1.0	Initial release.