AN 023: Using the Trion Power Estimator

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Contents

Introduction

Designing low-power systems has become increasingly important. Battery-powered, handheld, IoT, and mobile applications are obvious power-sensitive systems. However, even in power-hungry systems, just a few percent of power savings can translate into significant operating cost reductions.

Each Trion® FPGA has its own unique power profile. Therefore, Efinix provides a power estimator for each family member. These tools are Excel spreadsheets with macros. You can select the desired Trion® FPGA power estimator file, add information about your design, and the estimator calculates the projected power consumption. However, you need a license to obtain the **Power Estimator** Excel file from Efinix Support Center.

Note: The power estimators are just that - an estimate. They are intended to help guide your decision-making process as you pick an FPGA and plan your design. You should verify the actual power consumption in your system.

Total Tab

The Total tab is where you provide high-level information about your target FPGA and your system's thermal profile. It also displays power estimation summaries. Spreadsheet cells with a blue background are either static or calculated. White cells are for user input.

Device Settings

Enter data about the FPGA you want to use in the Device Settings table. Different FPGAs consume different amounts of power for the same design. For example, a larger FPGA consumes more power than a smaller one.

Table 1: Device Settings

Option	Choices	Notes
Package	Dependent on the FPGA	The package size affects the thermal resistance. The number of tabs in the spreadsheet changes based on the package you choose. For example, the T20 BGA256 does not have a MIPI interface, so that tab disappears when you choose that package.
Grade	Commercial, Industrial	Commercial is 0 to 85 °C. Industrial is -40 to 100 °C.
Condition	Typical, Maximum	Choose the static leakage power to mimic. Typical is the average expected leakage. Maximum is the worst case leakage.
Voltage Variation	Minimum, Maximum, Nominal (default)	Voltage domain for the FPGA. Choose maximum for the worst-case power estimation.

Thermal Profile

The estimator performs thermal analysis based on the FPGA you choose, the ambient temperature, and the airflow. The FPGA itself is a heat source, so the ambient temperature while it is operating, and the amount of cooling, if any, affects the overall power consumption.

The estimator calculates the effective Θ_{JA} and junction temperature based on your selections.

Table 2: Thermal Profile

Option	Choices	Notes
Ambient Temperature (°C)	User defined.	Enter the ambient temperature under which you expect your system to operate. Efinix recommends that you do not operate the FPGA at temperatures higher than the shown maximum ambient temperature.
Airflow	0.0 m/s, 1.0 m/s, 2.5 m/s	Choose the rate of air flowing in the system that reaches the FPGA. 0.0 is still air. A higher airflow lowers the junction to air thermal resistance and therefore lowers the junction temperature.
Board Thermal Profile	JEDEC (2s2p)	This is the profile that Efinix has modeled.
Cooling Solution	None, Custom	This option is available for larger packages. If you choose **Custom**, the **Effective Theta-JA (°C/W)** option is editable.
Effective Theta-JA (°C/W)	Default or user defined.	If you select **Custom** as the Cooling Solution, you can then specify a value for this option. Otherwise, the estimator calculates it for you.

The **Notes** field shows warning messages if the junction temperature exceeds the user selected operating temperature range or if there is a thermal runaway causing the leakage power to never converge.

Power Supply Summary

The Power Supply Summary table shows the estimated current consumption in mA for each voltage domain for the resource utilization you specify. This summary includes static, DC, and dynamic power consumption. These values help you to determine the specifications for the power regulator to use on your board.

Block Power Summary

The Block Power Summary table shows the DC and dynamic power consumption totals from the other tabs in the worksheet.

The static power shows the leakage power, which is a combination of the thermal profile parameters and the selected FPGA.

The total power shows the DC power + dynamic power + static power.

Logic, Memory, and Multiplier Tabs

Your design will have at least one, and probably more, modules. To get a better power estimation, list the modules, their clock frequency, number of look-up tables (LUTs), number of flip-flops, number of memory blocks, and number of Multiplier on these tabs.

If you already have an Efinity design, you can obtain this data from the Module Resource Usage Distribution Estimates section in the **<*project*>.map.rpt** file.

Tip: Click on the column heading to view pop-up help.

About the Toggle Percentage

The AF column represents the average percentage of logic that toggles on each clock cycle. The default, 12.5%, is an industry accepted average. You can adjust the toggle rate higher, or lower, based on the operation you expect for the module.

Clock Tab

Power consumption is strongly correlated to the clock usage. On this tab you enter the clocks, their frequency, and the fanout, which is the total number of flip-flops fed by the clock.

If you already have an Efinity design, you can obtain this data from the synthesis report file.

Below is an example snippet from the Trion T120 BGA324 Raspberry Pi to HDMI report file. The Flip-Flops field in the report represents the number of fanout from a clock.

```
### ### Clock Load Distribution Report (begin) ### ###

      Clock     Flip-Flops   Memory Ports    Multipliers
      -----     ----------   ------------    -----------
    axi_clk           2417             78              0
 tx_slowclk           2279            200              0
  mipi_pclk             83             20              0
   i_sysclk            203              3              0

### ### Clock Load Distribution Report (end) ### ###
```

IO Tab

Trion® I/O pins support several I/O standards. You use this tab to summarize how many input, output, and inout (bidirectional) pins your design uses.

The estimator only needs you to enter the number of input pins for 3.3 V LVDS. The input pin power consumption for the other standards is negligible.

For the 3.3 V LVDS standard, the drive setting represents the LVDS Output Load you select in the Efinity® Interface Designer:

- 0 for 3 pF
- 1 for 5 pF
- 2 for 7 pF
- 3 for 10 pF

You can specify the data rate: single data rate (SDR) or double data rate I/O (DDR). In Efinity® report files, pins that use double data rate I/O are indicated as `DDIO`.

For output and inout pins, enter the pin loading (in pF) in the Load (pf) cell or use the default, which is 1.2. This value is the total load, including the die capacitance + package capacitance + board (off chip) capacitance. For general estimation, the die + package capacitance is about 1 - 2 pF; can use 2 to be more conservative. So if your off-chip capacitance is 10 pF, you would enter 12 pF (2 + 10) in the Load cell.

The Output Enable column represents that average percentage of time that the output pins are enabled and inout pins are outputs and enabled. The default is 100%.

You can also adjust the AF percentage. See **About the Toggle Percentage** on page 5

PLL Tab

The PLL tab captures data about the PLLs your design uses. Enter the output frequency and VCO frequency for each PLL.

Table 3: Frequency Settings

Setting	Description
Output Clock Frequency (MHz)	In this column, insert the highest value of the output clock frequency. For example, if you have three PLL output clocks, 10 MHz, 20 MHz, and 50 MHz, use the **50**. Valid values are 0.24 to 500.
VCO Frequency (MHz)	Insert a number between 500 and 1600.

MIPI Tab

In the MIPI tab, enter the information about the MIPI interfaces that your design uses. Specify the number of channels (MIPI block x4 data lanes only), whether it is TX or RX, and the data rate.

You can also indicate the amount of time that the MIPI interface is operating in high-speed mode. The default is 12.5%.

In this tab, the AF% represents the activity of the user data stream. The default is 12.5%, but you can set another value based on your design's operation.

DDR Tab

The DDR tab contains data about the DDR interface. Specify:

- *DDR type*—DDR3, DDR3L, LPDDR2, LPDDR3.
- *DQ width*—x8, x16, or x32, the choice varies based on the FPGA and package you choose.
- *AXI interface*—This is the width of the interface, either 128 or 256 depending on the FPGA, package, and AXI interface you choose.

You can also indicate the amount of time that the DDR interface is operating in read mode. The default is 50%.

Revision History

Table 4: Revision History

Date	Version	Description
September 2022	1.3	Added-in info on how and where to obtain power estimator file in Introduction section. (DOC-882)
March 2022	1.2	Updated the filename that contains Module Resource Usage Distribution Estimates. (DOC-682)
March 2021	1.1	Clarified the settings in the PLL tab. (DOC-414)
July 2020	1.0	Initial release.