



AN 019: Trion[®] Pin Migration Guide

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Introduction

Trion® FPGAs are available in a variety of densities and packages. You can migrate your project from one FPGA to another to ease the design process. For example, you can target a larger device for debugging and then move to a smaller one for production. The new FPGA you select may not have the same features as the existing one, and some resources may not have the same names.

There are three methods to perform the migration depending on the Efinity® software version and the device package you are migrating to.

Table 1: Trion® FPGA Migration Methods

Efinity® Version	FPGA Package Migration	Migration Method
2020.2 or later	Migrating to similar package	Automatic Migration
	Migrating to different package	Migrate Design Wizard
2020.1 or older	Migrating to similar package except between Trion® T20/T35 and Trion® T55/T85/T120 FPGAs in BGA324	Automatic Migration
	Migrating between Trion® T20/T35 and Trion® T55/T85/T120 FPGAs in BGA324	Manual Migration ⁽¹⁾
	Migrating to different package	Manual Migration

Automatic Migration

When you choose a new FPGA in the Project Editor, the Efinity® software automatically performs a design check in the background to help you migrate the design.

If the new FPGA you choose is similar to the existing one (for example, you want to change from the T13 in the BGA256 to the T20 in the BGA256), the software can migrate all the assignments automatically and gives a message that migration completed successfully. You do not need to do anything else.

⁽¹⁾ Use the provided .csv template to perform migration.

Migrate Design Wizard

If the software cannot migrate automatically, it launches the Migrate Design wizard. This wizard helps you decide how to handle the changes. In the first pane, the wizard:

- Shows the issues it found, for example, GPIO feature differences.
- Asks if you want to create a new interface design or update your current one.
- Lets you back up your existing interface design so you can go back to it if needed.

Figure 1: Migrate Design Wizard First Pane

Migrate Design

You have changed the design's FPGA from T120F576 to T85F484. Also, the following are additional highlights:
Unsupported_block: MIPI.

You can create a new interface design, migrate the existing design to the new device, or cancel.

Migration Action

☐ Create New Design ☒ Update Existing Design

☒ Enable Design Backup

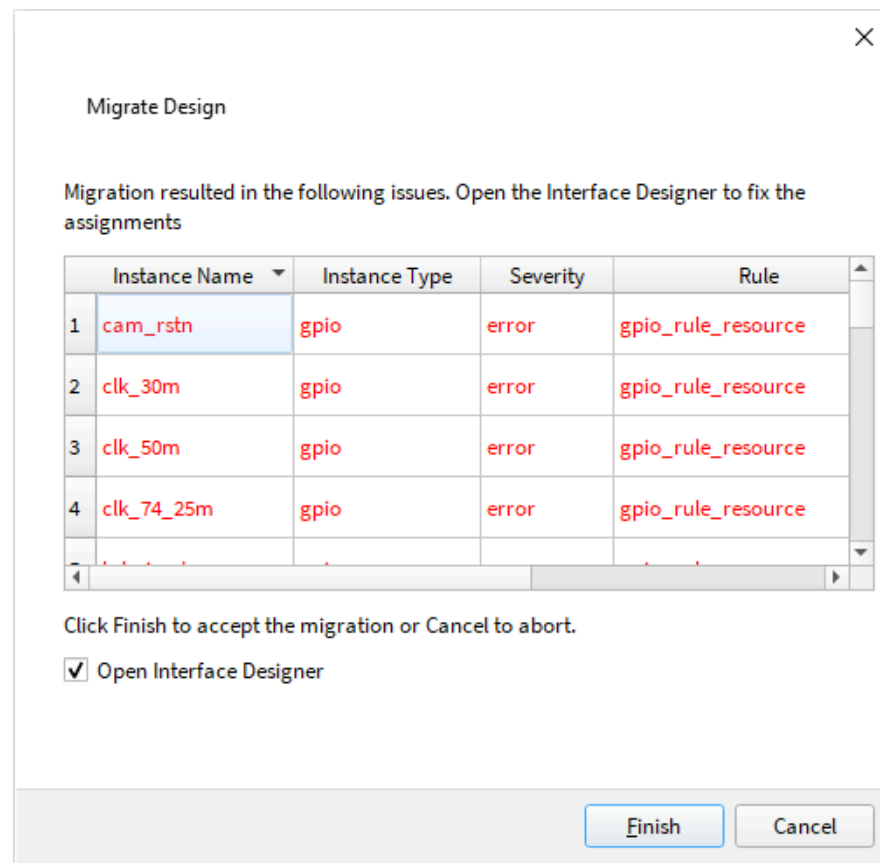
If you choose to migrate, you can specify an optional back-up filename for the existing design.

Filename

Location

In the second pane, the wizard shows the assignments that have problems. If you decide to continue migration, the wizard opens the Interface Designer so you can fix the problems. You can also cancel to stop migration.

Figure 2: Migrate Design Wizard Second Pane



Note: If you cancel migration and keep the new FPGA setting, the Migrate Design wizard opens again the next time you run the Interface Designer.

Manual Migration

When migrating between FPGAs with different packages in Efinity® 2020.1 or older, you need to manually migrate your design by manually assigning the pins in the Interface Designer.

Migration between Trion® T20/T35 and Trion® T55/T85/T120 FPGAs in BGA324 packages in Efinity® 2020.1 or older also requires a manual migration process. Efinix provides **.csv** template files to help you with the pin migration as described in the following sections.

Pin Migration Guidelines

The FPGA pins are grouped into four categories for migration purposes. The following table explains the pin migration guidelines for each pin category.

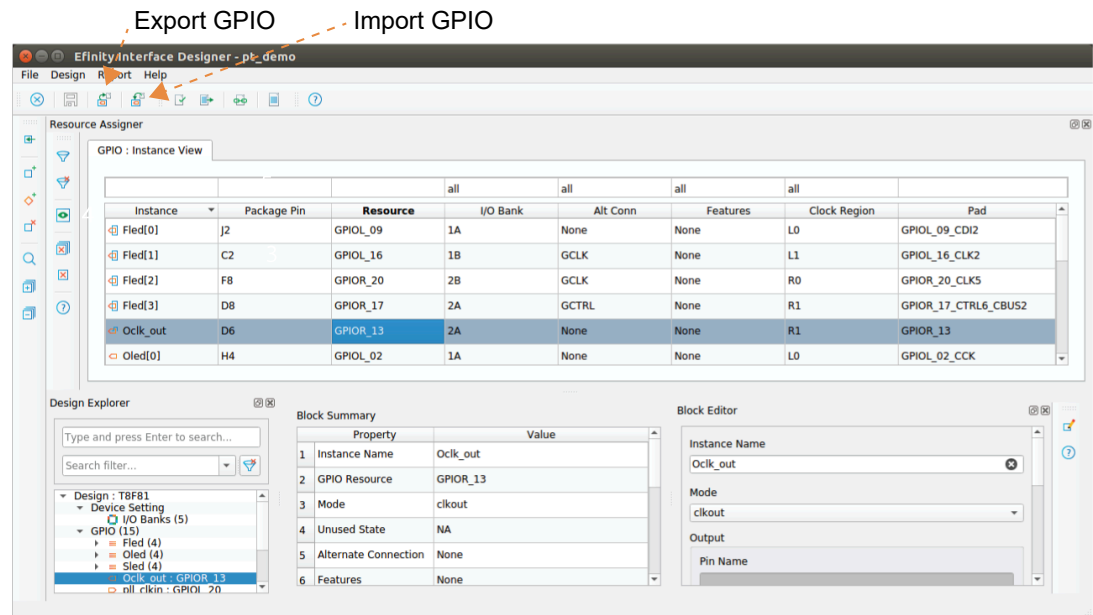
Table 2: Pin Migration Guidelines for Different Pin Categories

Pin Category	Description	Migration Guideline
1	These pins have the same package pins and pin names. Table 3: Category 1 Pin on page 9	No action is required.
2	VCCIO and REF_RES pins have different pin names but the same package pins and matched the corresponding bank for the I/O pins. Table 4: Category 2 Pin on page 15	No action is required.
3	These pins have different pin names, but they have the same functionality and package pin. Table 5: Category 3 Pin on page 16	Ensure that the pin names assigned in the Interface Designer are correct.
4	These pins can be assigned as PLL reference clock inputs in Trion® T20/T35 FPGAs, but not in Trion® T55/T85/T120 FPGAs. Table 6: Category 4 Pin on page 18	Migrating Trion® T55/T85/T120 to Trion® T20/T35: No action is required. Migrating Trion® T20/T35 to Trion® T55/T85/T120: If you assigned them as PLL reference clock input, reassign it to other reference clock input.

Migrating the Pins

Some of the package pins have different pin names between Trion® T20/T35 and Trion® T55/T85/T120 FPGAs. This task renames the pin based on the target migration using the **Import GPIO** and **Export GPIO** features in Efinity® Interface Designer.

Figure 3: Resource Assigner GUI



Follow these steps to migrate your pin out:

1. Open your existing design in Efinity® software.
2. Open the Efinity® **Interface Designer**, click **Export GPIO** and fill in the **File Name** and **Location** then click **OK**.
3. Close the **Interface Designer**.
4. Open the exported GPIO .csv file.
5. Download and open the following pin-out template in a spreadsheet program:
 - Migrating from Trion® T55/T85/T120 to Trion® T20/T35:
[t35f324_pinout_template.csv](#)
 - Migrating from Trion® T20/T35 to Trion® T55/T85/T120:
[t120f324_pinout_template.csv](#)

- Copy the first column of the pin-out template and replace the first column of exported GPIO file. Save the exported GPIO file.

Step 1: Copy this column.



Step 2: Paste to this column.



A		A	
1	# Efinity GPIO Pin Assignment	1	# Efinity GPIO Pin Assignment
2	# Version: 2019.3.272	2	# Version: 2019.3.272
3	# Date: 2020-01-20 10:27	3	# Date: 2020-03-23 11:18
4	#	4	#
5	# Copyright (C) 2017 - 2019 Efinix Inc. All rights reserved.	5	# Copyright (C) 2017 - 2019 Efinix Inc. All rights reserved.
6	#	6	#
7	# Device: T120F324	7	# Device: T35F324
8	# Package: 324-ball FBGA (preliminary)	8	# Package: 324-ball FBGA (preliminary)
9	# Project: helloworld	9	# Project: helloworld
10	# Configuration mode: active (x1)	10	# Configuration mode: active (x1)
11	# Timing Model: C4 (preliminary)	11	# Timing Model: C4 (preliminary)
12	Package Pin-Pad Name	12	Package Pin-Pad Name
13	R17-GPIOB_TXN00	13	R17-GPIOB_TXN00
14	T18-GPIOB_TXN01	14	T18-GPIOB_TXN01
15	P18-GPIOB_TXN02	15	P18-GPIOB_TXN02
16	V16-GPIOB_TXN03_CDI30	16	V16-GPIOB_TXN03_CDI30
17	V15-GPIOB_TXN04_CDI28	17	V15-GPIOB_TXN04_CDI28
18	R15-GPIOB_TXN05_CDI26	18	R15-GPIOB_TXN05_CDI26
19	U14-GPIOB_TXN06_CDI24	19	U14-GPIOB_TXN06_CDI24
20	R14-GPIOB_TXN07_CDI22	20	R14-GPIOB_TXN07_CDI22

Pin-out template file
Exported GPIO file

- In the Efinity[®] software, go to **File > Edit Project...**
- Click **Select**, choose the Trion[®] FPGA that you are migrating to and click **OK**.
- Open the **Interface Designer**, and click **Update Design** in the **Device Change Detected** message window.



Note: Ignore all error messages when opening the **Interface Designer**.

- Click **Import GPIO**, select the modified GPIO file and click **Next**.
- Click **Finish** when the **Interface Designer** prompts message stating that no issue are found when checking the file to be imported.

Appendix: Pin Category List

Table 3: Category 1 Pin

These pins have the same package pins and pin names.

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
A1	-	GND	-	GND
A18	-	GND	-	GND
C12	-	GND	-	GND
C15	-	GND	-	GND
D10	-	GND	-	GND
F17	-	GND	-	GND
F4	-	GND	-	GND
G11	-	GND	-	GND
G7	-	GND	-	GND
G9	-	GND	-	GND
H1	-	GND	-	GND
H10	-	GND	-	GND
H12	-	GND	-	GND
H8	-	GND	-	GND
J11	-	GND	-	GND
J16	-	GND	-	GND
J7	-	GND	-	GND
J9	-	GND	-	GND
K10	-	GND	-	GND
K12	-	GND	-	GND
K8	-	GND	-	GND
L11	-	GND	-	GND
L7	-	GND	-	GND
L9	-	GND	-	GND
M1	-	GND	-	GND
M10	-	GND	-	GND
M12	-	GND	-	GND
M5	-	GND	-	GND
M8	-	GND	-	GND
N16	-	GND	-	GND
P7	-	GND	-	GND
R10	-	GND	-	GND

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
R2	-	GND	-	GND
R4	-	GND	-	GND
T13	-	GND	-	GND
V1	-	GND	-	GND
V18	-	GND	-	GND
V4	-	GND	-	GND
C3	-	GNDA_MIP1	-	GNDA_MIP1
C7	-	GNDA_MIP1	-	GNDA_MIP1
C8	-	GNDA_MIP1	-	GNDA_MIP1
F2	-	GNDA_MIP1	-	GNDA_MIP1
G10	-	VCC	-	VCC
G12	-	VCC	-	VCC
G8	-	VCC	-	VCC
H11	-	VCC	-	VCC
H7	-	VCC	-	VCC
H9	-	VCC	-	VCC
J10	-	VCC	-	VCC
J12	-	VCC	-	VCC
J8	-	VCC	-	VCC
K11	-	VCC	-	VCC
K7	-	VCC	-	VCC
K9	-	VCC	-	VCC
L10	-	VCC	-	VCC
L12	-	VCC	-	VCC
L8	-	VCC	-	VCC
M11	-	VCC	-	VCC
M7	-	VCC	-	VCC
M9	-	VCC	-	VCC
C5	-	VCC12A_MIP10_RX	-	VCC12A_MIP10_RX
C6	-	VCC12A_MIP10_TX	-	VCC12A_MIP10_TX
H3	-	VCC12A_MIP11_RX	-	VCC12A_MIP11_RX
C2	-	VCC12A_MIP11_TX	-	VCC12A_MIP11_TX
D7	-	VCC25A_MIP10	-	VCC25A_MIP10
C4	-	VCC25A_MIP11	-	VCC25A_MIP11
F12	-	VCCA_BL	-	VCCA_BL
N8	-	VCCA_BR	-	VCCA_BR
P8	-	VCCA_BR	-	VCCA_BR

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
F8	-	VCCA_TR	-	VCCA_TR
F9	-	VCCA_TR	-	VCCA_TR
J2	-	VCCIO_DDR	-	VCCIO_DDR
K4	-	VCCIO_DDR	-	VCCIO_DDR
L2	-	VCCIO_DDR	-	VCCIO_DDR
L6	-	VCCIO_DDR	-	VCCIO_DDR
P2	-	VCCIO_DDR	-	VCCIO_DDR
P5	-	VCCIO_DDR	-	VCCIO_DDR
T7	-	VCCIO_DDR	-	VCCIO_DDR
U2	-	VCCIO_DDR	-	VCCIO_DDR
U5	-	VCCIO_DDR	-	VCCIO_DDR
L13	-	VCCIO1A	-	VCCIO1A
K13	-	VCCIO1B_1C	-	VCCIO1B_1C
N18	BANK1A	CDONE	BANK1A	CDONE
N17	BANK1A	CRESET_N	BANK1A	CRESET_N
P15	BANK1A	GPIOL_00_SS_N	BANK1A	GPIOL_00_SS_N
N13	BANK1A	GPIOL_01_CCK	BANK1A	GPIOL_01_CCK
N15	BANK1A	GPIOL_04_CSI	BANK1A	GPIOL_04_CSI
M15	BANK1A	GPIOL_05_CSO	BANK1A	GPIOL_05_CSO
M13	BANK1A	GPIOL_08_CDI0	BANK1A	GPIOL_08_CDI0
N14	BANK1A	GPIOL_09_CDI1	BANK1A	GPIOL_09_CDI1
M14	BANK1A	GPIOL_11_CBUS0	BANK1A	GPIOL_11_CBUS0
M16	BANK1A	GPIOL_12_CBUS1	BANK1A	GPIOL_12_CBUS1
M17	BANK1A	GPIOL_13_CBUS2	BANK1A	GPIOL_13_CBUS2
T16	BANK1A	TCK	BANK1A	TCK
R16	BANK1A	TDI	BANK1A	TDI
P17	BANK1A	TDO	BANK1A	TDO
P16	BANK1A	TMS	BANK1A	TMS
K14	BANK1B	GPIOL_14_CDI2	BANK1B	GPIOL_14_CDI2
L14	BANK1B	GPIOL_15_PLLIN0	BANK1B	GPIOL_15_PLLIN0
K18	BANK1B	GPIOL_16_CDI3	BANK1B	GPIOL_16_CDI3
L15	BANK1B	GPIOL_17_EXTFB0	BANK1B	GPIOL_17_EXTFB0
M18	BANK1B	GPIOL_18_CDI4	BANK1B	GPIOL_18_CDI4
L18	BANK1B	GPIOL_20_CDI5	BANK1B	GPIOL_20_CDI5
L16	BANK1B	GPIOL_22_CDI6	BANK1B	GPIOL_22_CDI6
L17	BANK1B	GPIOL_24_CDI7	BANK1B	GPIOL_24_CDI7
K16	BANK1C	GPIOL_62_CTRL0	BANK1C	GPIOL_62_CTRL0

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
K15	BANK1C	GPIOL_63_CTRL1	BANK1C	GPIOL_63_CTRL1
K17	BANK1C	GPIOL_66_CLK0	BANK1C	GPIOL_66_CLK0
H14	BANK1D	GPIOL_72_CLK6	BANK1D	GPIOL_72_CLK6
H13	BANK1D	GPIOL_73_CLK7	BANK1D	GPIOL_73_CLK7
G13	BANK1D	GPIOL_75_CTRL5	BANK1D	GPIOL_75_CTRL5
D5	BANK3A	MIPI0_RXDN0	BANK3A	MIPI0_RXDN0
D8	BANK3A	MIPI0_RXDN1	BANK3A	MIPI0_RXDN1
F5	BANK3A	MIPI0_RXDN2	BANK3A	MIPI0_RXDN2
D6	BANK3A	MIPI0_RXDN3	BANK3A	MIPI0_RXDN3
F7	BANK3A	MIPI0_RXDN4	BANK3A	MIPI0_RXDN4
E5	BANK3A	MIPI0_RXDP0	BANK3A	MIPI0_RXDP0
E8	BANK3A	MIPI0_RXDP1	BANK3A	MIPI0_RXDP1
F6	BANK3A	MIPI0_RXDP2	BANK3A	MIPI0_RXDP2
E6	BANK3A	MIPI0_RXDP3	BANK3A	MIPI0_RXDP3
E7	BANK3A	MIPI0_RXDP4	BANK3A	MIPI0_RXDP4
A6	BANK3A	MIPI0_TXDN0	BANK3A	MIPI0_TXDN0
B7	BANK3A	MIPI0_TXDN1	BANK3A	MIPI0_TXDN1
A8	BANK3A	MIPI0_TXDN2	BANK3A	MIPI0_TXDN2
B5	BANK3A	MIPI0_TXDN3	BANK3A	MIPI0_TXDN3
B4	BANK3A	MIPI0_TXDN4	BANK3A	MIPI0_TXDN4
B6	BANK3A	MIPI0_TXDP0	BANK3A	MIPI0_TXDP0
A7	BANK3A	MIPI0_TXDP1	BANK3A	MIPI0_TXDP1
B8	BANK3A	MIPI0_TXDP2	BANK3A	MIPI0_TXDP2
A5	BANK3A	MIPI0_TXDP3	BANK3A	MIPI0_TXDP3
A4	BANK3A	MIPI0_TXDP4	BANK3A	MIPI0_TXDP4
E4	BANK3B	MIPI1_RXDN0	BANK3B	MIPI1_RXDN0
G3	BANK3B	MIPI1_RXDN1	BANK3B	MIPI1_RXDN1
F1	BANK3B	MIPI1_RXDN2	BANK3B	MIPI1_RXDN2
G2	BANK3B	MIPI1_RXDN3	BANK3B	MIPI1_RXDN3
E3	BANK3B	MIPI1_RXDN4	BANK3B	MIPI1_RXDN4
D4	BANK3B	MIPI1_RXDP0	BANK3B	MIPI1_RXDP0
F3	BANK3B	MIPI1_RXDP1	BANK3B	MIPI1_RXDP1
G1	BANK3B	MIPI1_RXDP2	BANK3B	MIPI1_RXDP2
H2	BANK3B	MIPI1_RXDP3	BANK3B	MIPI1_RXDP3
D3	BANK3B	MIPI1_RXDP4	BANK3B	MIPI1_RXDP4
A3	BANK3B	MIPI1_TXDN0	BANK3B	MIPI1_TXDN0
A2	BANK3B	MIPI1_TXDN1	BANK3B	MIPI1_TXDN1

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
B1	BANK3B	MIPI1_TXDN2	BANK3B	MIPI1_TXDN2
E2	BANK3B	MIPI1_TXDN3	BANK3B	MIPI1_TXDN3
D1	BANK3B	MIPI1_TXDN4	BANK3B	MIPI1_TXDN4
B3	BANK3B	MIPI1_TXDP0	BANK3B	MIPI1_TXDP0
B2	BANK3B	MIPI1_TXDP1	BANK3B	MIPI1_TXDP1
C1	BANK3B	MIPI1_TXDP2	BANK3B	MIPI1_TXDP2
D2	BANK3B	MIPI1_TXDP3	BANK3B	MIPI1_TXDP3
E1	BANK3B	MIPI1_TXDP4	BANK3B	MIPI1_TXDP4
P3	BANK3D	DDR_A[0]	BANK3E	DDR_A[0]
P4	BANK3D	DDR_A[1]	BANK3E	DDR_A[1]
V7	BANK3D	DDR_A[10]	BANK3E	DDR_A[10]
U7	BANK3D	DDR_A[11]	BANK3E	DDR_A[11]
U6	BANK3D	DDR_A[12]	BANK3E	DDR_A[12]
T6	BANK3D	DDR_A[13]	BANK3E	DDR_A[13]
V6	BANK3D	DDR_A[14]	BANK3E	DDR_A[14]
V5	BANK3D	DDR_A[15]	BANK3E	DDR_A[15]
R6	BANK3D	DDR_A[2]	BANK3E	DDR_A[2]
P6	BANK3D	DDR_A[3]	BANK3E	DDR_A[3]
T1	BANK3D	DDR_A[4]	BANK3E	DDR_A[4]
R3	BANK3D	DDR_A[5]	BANK3E	DDR_A[5]
R7	BANK3D	DDR_A[6]	BANK3E	DDR_A[6]
V8	BANK3D	DDR_A[7]	BANK3E	DDR_A[7]
T4	BANK3D	DDR_A[8]	BANK3E	DDR_A[8]
T3	BANK3D	DDR_A[9]	BANK3E	DDR_A[9]
T5	BANK3D	DDR_BA[0]	BANK3E	DDR_BA[0]
U3	BANK3D	DDR_BA[1]	BANK3E	DDR_BA[1]
R5	BANK3D	DDR_BA[2]	BANK3E	DDR_BA[2]
V2	BANK3D	DDR_CAS_N	BANK3E	DDR_CAS_N
P1	BANK3D	DDR_CK	BANK3E	DDR_CK
R1	BANK3D	DDR_CK_N	BANK3E	DDR_CK_N
N7	BANK3D	DDR_CKE	BANK3E	DDR_CKE
N6	BANK3D	DDR_CS_N	BANK3E	DDR_CS_N
L1	BANK3D	DDR_DM[0]	BANK3E	DDR_DM[0]
H5	BANK3D	DDR_DM[1]	BANK3E	DDR_DM[1]
N4	BANK3D	DDR_DQ[0]	BANK3E	DDR_DQ[0]
N2	BANK3D	DDR_DQ[1]	BANK3E	DDR_DQ[1]
J3	BANK3D	DDR_DQ[10]	BANK3E	DDR_DQ[10]

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
K3	BANK3D	DDR_DQ[11]	BANK3E	DDR_DQ[11]
J4	BANK3D	DDR_DQ[12]	BANK3E	DDR_DQ[12]
H4	BANK3D	DDR_DQ[13]	BANK3E	DDR_DQ[13]
J5	BANK3D	DDR_DQ[14]	BANK3E	DDR_DQ[14]
G4	BANK3D	DDR_DQ[15]	BANK3E	DDR_DQ[15]
N1	BANK3D	DDR_DQ[2]	BANK3E	DDR_DQ[2]
M2	BANK3D	DDR_DQ[3]	BANK3E	DDR_DQ[3]
M4	BANK3D	DDR_DQ[4]	BANK3E	DDR_DQ[4]
L3	BANK3D	DDR_DQ[5]	BANK3E	DDR_DQ[5]
K1	BANK3D	DDR_DQ[6]	BANK3E	DDR_DQ[6]
L4	BANK3D	DDR_DQ[7]	BANK3E	DDR_DQ[7]
J1	BANK3D	DDR_DQ[8]	BANK3E	DDR_DQ[8]
K2	BANK3D	DDR_DQ[9]	BANK3E	DDR_DQ[9]
M3	BANK3D	DDR_DQS[0]	BANK3E	DDR_DQS[0]
K5	BANK3D	DDR_DQS[1]	BANK3E	DDR_DQS[1]
N3	BANK3D	DDR_DQS_N[0]	BANK3E	DDR_DQS_N[0]
L5	BANK3D	DDR_DQS_N[1]	BANK3E	DDR_DQS_N[1]
U1	BANK3D	DDR_ODT	BANK3E	DDR_ODT
V3	BANK3D	DDR_RAS_N	BANK3E	DDR_RAS_N
T2	BANK3D	DDR_RST_N	BANK3E	DDR_RST_N
M6	BANK3D	DDR_VREF	BANK3E	DDR_VREF
U4	BANK3D	DDR_WE_N	BANK3E	DDR_WE_N
N5	BANK3D	DDR_ZQ	BANK3E	DDR_ZQ
U12	BANK4A	GPIOB_TXN10	BANK4E	GPIOB_TXN10
T12	BANK4A	GPIOB_TXN11	BANK4E	GPIOB_TXN11
N12	BANK4A	GPIOB_TXN12	BANK4E	GPIOB_TXN12
P11	BANK4A	GPIOB_TXN13_CDI18	BANK4E	GPIOB_TXN13_CDI18
P10	BANK4A	GPIOB_TXN14_CDI16	BANK4E	GPIOB_TXN14_CDI16
V10	BANK4A	GPIOB_TXN15_CDI14	BANK4E	GPIOB_TXN15_CDI14
P9	BANK4A	GPIOB_TXN16_CDI12	BANK4E	GPIOB_TXN16_CDI12
U9	BANK4A	GPIOB_TXN17_CDI10	BANK4E	GPIOB_TXN17_CDI10
T11	BANK4A	GPIOB_TXN18_CDI8	BANK4E	GPIOB_TXN18_CDI8
R9	BANK4A	GPIOB_TXN19	BANK4E	GPIOB_TXN19
V12	BANK4A	GPIOB_TXP10	BANK4E	GPIOB_TXP10
R12	BANK4A	GPIOB_TXP11	BANK4E	GPIOB_TXP11
P12	BANK4A	GPIOB_TXP12	BANK4E	GPIOB_TXP12
N11	BANK4A	GPIOB_TXP13_CDI19	BANK4E	GPIOB_TXP13_CDI19

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
N10	BANK4A	GPIOB_TXP14_EXTFB1_CDI17	BANK4E	GPIOB_TXP14_CDI17
N9	BANK4A	GPIOB_TXP16_CDI13	BANK4E	GPIOB_TXP16_CDI13
V9	BANK4A	GPIOB_TXP17_CDI11	BANK4E	GPIOB_TXP17_CDI11
U11	BANK4A	GPIOB_TXP18_EXTFB2_CDI9	BANK4E	GPIOB_TXP18_CDI9
R17	BANK4B	GPIOB_TXN00	BANK4F	GPIOB_TXN00
T18	BANK4B	GPIOB_TXN01	BANK4F	GPIOB_TXN01
P18	BANK4B	GPIOB_TXN02	BANK4F	GPIOB_TXN02
V16	BANK4B	GPIOB_TXN03_CDI30	BANK4F	GPIOB_TXN03_CDI30
V15	BANK4B	GPIOB_TXN04_CDI28	BANK4F	GPIOB_TXN04_CDI28
R15	BANK4B	GPIOB_TXN05_CDI26	BANK4F	GPIOB_TXN05_CDI26
U14	BANK4B	GPIOB_TXN06_CDI24	BANK4F	GPIOB_TXN06_CDI24
R14	BANK4B	GPIOB_TXN07_CDI22	BANK4F	GPIOB_TXN07_CDI22
U13	BANK4B	GPIOB_TXN08_CDI20	BANK4F	GPIOB_TXN08_CDI20
R13	BANK4B	GPIOB_TXN09	BANK4F	GPIOB_TXN09
T17	BANK4B	GPIOB_TXP00	BANK4F	GPIOB_TXP00
U18	BANK4B	GPIOB_TXP01	BANK4F	GPIOB_TXP01
R18	BANK4B	GPIOB_TXP02	BANK4F	GPIOB_TXP02
U16	BANK4B	GPIOB_TXP03_CDI31	BANK4F	GPIOB_TXP03_CDI31
U15	BANK4B	GPIOB_TXP04_CDI29	BANK4F	GPIOB_TXP04_CDI29
T15	BANK4B	GPIOB_TXP05_CDI27	BANK4F	GPIOB_TXP05_CDI27
V14	BANK4B	GPIOB_TXP06_CDI25	BANK4F	GPIOB_TXP06_CDI25
P14	BANK4B	GPIOB_TXP07_CDI23	BANK4F	GPIOB_TXP07_CDI23
V13	BANK4B	GPIOB_TXP08_EXTFB0_CDI21	BANK4F	GPIOB_TXP08_CDI21

Table 4: Category 2 Pin

VCCIO and REF_RES pins have different pin names but the same package pins and matched the corresponding bank for the I/O pins.

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Names	Bank Number	Pin Names
J13	-	VCCIO1D_1E	-	VCCIO1D_1E_1F_1G
E10	-	VCCIO2A	-	VCCIO2D
F15	-	VCCIO2A	-	VCCIO2D
C17	-	VCCIO2B	-	VCCIO2E
F18	-	VCCIO2B	-	VCCIO2E
C10	-	VCCIO2C	-	VCCIO2F
C14	-	VCCIO2C	-	VCCIO2F
J6	-	VCCIO3C_TR_BR	-	VCCIO3D_TR_BR

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Names	Bank Number	Pin Names
R11	-	VCCIO4A	-	VCCIO4E
T10	-	VCCIO4A	-	VCCIO4E
T14	-	VCCIO4B	-	VCCIO4F
U17	-	VCCIO4B	-	VCCIO4F
V11	BANK4A	REF_RES_4A	BANK4E	REF_RES_4E
V17	BANK4B	REF_RES_4B	BANK4F	REF_RES_4F

Table 5: Category 3 Pin

These pins have different pin names, but they have the same functionality and package pin.

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
J14	BANK1E	GPIOL_102_NSTATUS	BANK1G	GPIOL_150_NSTATUS
J15	BANK1E	GPIOL_103_TEST_N	BANK1G	GPIOL_151_TEST_N
J17	BANK1E	GPIOL_108_CBSEL0	BANK1G	GPIOL_156_CBSEL0
J18	BANK1E	GPIOL_109_CBSEL1	BANK1G	GPIOL_157_CBSEL1
C13	BANK2A	GPIOT_RXN00	BANK2D	GPIOT_RXN01
D16	BANK2A	GPIOT_RXN01	BANK2D	GPIOT_RXN02
C11	BANK2A	GPIOT_RXN02	BANK2D	GPIOT_RXN03
E15	BANK2A	GPIOT_RXN03	BANK2D	GPIOT_RXN04
E14	BANK2A	GPIOT_RXN04	BANK2D	GPIOT_RXN05
D12	BANK2A	GPIOT_RXN05	BANK2D	GPIOT_RXN06
F13	BANK2A	GPIOT_RXN06	BANK2D	GPIOT_RXN07
F11	BANK2A	GPIOT_RXN07_EXTFB0	BANK2D	GPIOT_RXN08_EXTFB0
F16	BANK2A	GPIOT_RXN08_CLKN0	BANK2D	GPIOT_RXN09_CLKN0
D13	BANK2A	GPIOT_RXP00	BANK2D	GPIOT_RXP01
C16	BANK2A	GPIOT_RXP01	BANK2D	GPIOT_RXP02
D11	BANK2A	GPIOT_RXP02	BANK2D	GPIOT_RXP03
D15	BANK2A	GPIOT_RXP03	BANK2D	GPIOT_RXP04
D14	BANK2A	GPIOT_RXP04	BANK2D	GPIOT_RXP05
E12	BANK2A	GPIOT_RXP05	BANK2D	GPIOT_RXP06
E13	BANK2A	GPIOT_RXP06	BANK2D	GPIOT_RXP07
E11	BANK2A	GPIOT_RXP07_EXTFB0	BANK2D	GPIOT_RXP08_EXTFB0
E16	BANK2A	GPIOT_RXP08_CLKP0	BANK2D	GPIOT_RXP09_CLKP0
H17	BANK2B	GPIOT_RXN09	BANK2E	GPIOT_RXN11
H16	BANK2B	GPIOT_RXN10	BANK2E	GPIOT_RXN12
H15	BANK2B	GPIOT_RXN11	BANK2E	GPIOT_RXN13
F14	BANK2B	GPIOT_RXN12	BANK2E	GPIOT_RXN14

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
E17	BANK2B	GPIOT_RXN13	BANK2E	GPIOT_RXN15
E18	BANK2B	GPIOT_RXN14	BANK2E	GPIOT_RXN16
G18	BANK2B	GPIOT_RXN15	BANK2E	GPIOT_RXN17
C18	BANK2B	GPIOT_RXN16_EXTFB1	BANK2E	GPIOT_RXN18_EXTFB1
B17	BANK2B	GPIOT_RXN17_CLKN1	BANK2E	GPIOT_RXN19_CLKN1
G17	BANK2B	GPIOT_RXP09	BANK2E	GPIOT_RXP11
G16	BANK2B	GPIOT_RXP10	BANK2E	GPIOT_RXP12
G15	BANK2B	GPIOT_RXP11	BANK2E	GPIOT_RXP13
G14	BANK2B	GPIOT_RXP12	BANK2E	GPIOT_RXP14
D17	BANK2B	GPIOT_RXP13	BANK2E	GPIOT_RXP15
D18	BANK2B	GPIOT_RXP14	BANK2E	GPIOT_RXP16
H18	BANK2B	GPIOT_RXP15	BANK2E	GPIOT_RXP17
B18	BANK2B	GPIOT_RXP16_EXTFB1	BANK2E	GPIOT_RXP18_EXTFB1
A17	BANK2B	GPIOT_RXP17_CLKP1	BANK2E	GPIOT_RXP19_CLKP1
A16	BANK2C	GPIOT_RXN18	BANK2F	GPIOT_RXN20
A15	BANK2C	GPIOT_RXN19	BANK2F	GPIOT_RXN21
A14	BANK2C	GPIOT_RXN20	BANK2F	GPIOT_RXN22
A13	BANK2C	GPIOT_RXN21	BANK2F	GPIOT_RXN23
B12	BANK2C	GPIOT_RXN22	BANK2F	GPIOT_RXN24
B11	BANK2C	GPIOT_RXN23	BANK2F	GPIOT_RXN27
B10	BANK2C	GPIOT_RXN24_EXTFB2	BANK2F	GPIOT_RXN28_EXTFB2
A9	BANK2C	GPIOT_RXN25_CLKN2	BANK2F	GPIOT_RXN29_CLKN2
B16	BANK2C	GPIOT_RXP18	BANK2F	GPIOT_RXP20
B15	BANK2C	GPIOT_RXP19	BANK2F	GPIOT_RXP21
B14	BANK2C	GPIOT_RXP20	BANK2F	GPIOT_RXP22
B13	BANK2C	GPIOT_RXP21	BANK2F	GPIOT_RXP23
A12	BANK2C	GPIOT_RXP22	BANK2F	GPIOT_RXP24
A11	BANK2C	GPIOT_RXP23	BANK2F	GPIOT_RXP27
A10	BANK2C	GPIOT_RXP24_EXTFB2	BANK2F	GPIOT_RXP28_EXTFB2
B9	BANK2C	GPIOT_RXP25_CLKP2	BANK2F	GPIOT_RXP29_CLKP2
G5	BANK3C	GPIOR_125_CTRL12	BANK3D	GPIOR_173_CTRL12
G6	BANK3C	GPIOR_126_CLK15	BANK3D	GPIOR_174_CLK15
H6	BANK3C	GPIOR_130_CLK11	BANK3D	GPIOR_178_CLK11
K6	BANK3C	GPIOR_135_CTRL10	BANK3D	GPIOR_183_CTRL10
U8	BR_CORNER	GPIOR_138_PLLIN0	BR_CORNER	GPIOR_186_PLLIN0
T8	BR_CORNER	GPIOR_139_PLLIN1	BR_CORNER	GPIOR_187_PLLIN1
R8	BR_CORNER	GPIOR_140_PLLIN2	BR_CORNER	GPIOR_188_PLLIN2

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
C9	TR_CORNER	GPIOR_118_PLLIN0	TR_CORNER	GPIOR_166_PLLIN0
D9	TR_CORNER	GPIOR_119_PLLIN1	TR_CORNER	GPIOR_167_PLLIN1
E9	TR_CORNER	GPIOR_120_PLLIN2	TR_CORNER	GPIOR_168_PLLIN2
F10	TR_CORNER	GPIOR_121_MREFCLK	TR_CORNER	GPIOR_169_MREFCLK

Table 6: Category 4 Pin

These pins can be assigned as PLL reference clock inputs in Trion® T20/T35 FPGAs, but not in Trion® T55/T85/T120 FPGAs.

Package Pin	Trion® T20/T35		Trion® T55/T85/T120	
	Bank Number	Pin Name	Bank Number	Pin Name
U10	BANK4A	GPIOB_TXP15_CLK1_CDI15	BANK4E	GPIOB_TXP15_CDI15
T9	BANK4A	GPIOB_TXP19_CLK2	BANK4E	GPIOB_TXP19
P13	BANK4B	GPIOB_TXP09_CLK0	BANK4F	GPIOB_TXP09

Revision History

Table 7: Document Revision History

Date	Version	Description
March 2021	2.0	Added automatic migration and migrate design wizard information.
March 2020	1.0	Initial release.