



# Topaz Tz170 J484 Development Kit User Guide

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# Introduction

Thank you for choosing the Topaz Tz170 J484 Development Kit (part number: Tz170J484-DK), which allows you to explore the features of the Tz170 FPGA.

The Topaz Tz170 J484 Development Kit lets you prototype designs for the Tz170 FPGA. The onboard memory has 256 Mbit memory that supports LPDDR4. The board has a variety of multi-purpose QSE connectors that work with Efinix daughter cards (available separately) or for your custom cards. Additionally, you can use the FMC connector with FPGA mezzanine cards to extend the board's functionality even further. Together these features help you prototype and design your high-volume application.



**Warning:** The board can be damaged without proper anti-static handling.

## What's in the Box?

The Topaz Tz170 J484 Development Kit includes:

- Topaz Tz170 J484 Development Board
- 1 USB type-C cable
- 12 V, 5 A universal power adapter
- 4 standoffs and 4 nuts

## Register Your Kit

When you purchase an Efinix development kit, you also receive a license for the Efinity<sup>®</sup> software, plus 1 year of software upgrades and patches. After the first year you can request a free maintenance renewal. The Efinity<sup>®</sup> software is available for download from the Support Center.

To download the software, first register at our Support Center (<https://www.efinixinc.com/register>), then register your development kit.

## Download the Efinity<sup>®</sup> Software

To develop your own designs for the Tz170 FPGA on the board, you must install the Efinity<sup>®</sup> software. You can obtain the software from the Efinix Support Center under Efinity Software ([www.efinixinc.com/support/](http://www.efinixinc.com/support/)).

The Efinity<sup>®</sup> software includes tools to program the device on the board. Refer to the Efinity<sup>®</sup> Software User Guide for information about how to program the device.



**Learn more:** Efinity<sup>®</sup> documentation is installed with the software (see **Help > Documentation**) and is also available in the Support Center under Documentation ([www.efinixinc.com/support/](http://www.efinixinc.com/support/)).

## Installing the Linux USB Driver

The following instructions explain how to install a USB driver for Linux operating systems.

1. Disconnect your board from your computer.
2. In a terminal, use these commands:

```
> sudo <installation directory>/bin/install_usb_driver.sh
> sudo udevadm control --reload-rules
> sudo udevadm trigger
```



**Note:** If your board was connected to your computer before you executed these commands, you need to disconnect it, then re-connect it.

## Installing the Windows USB Drivers

The Topaz Tz170 J484 Development Board has an FTDI FT2232H chip to communicate with the USB port.



**Note:** If you have another Efinix board and are using the Topaz Tz170 J484 Development Board, you must manage drivers accordingly. Refer to [AN 050: Managing Windows Drivers](#) for more information.

On Windows, you use software from Zadig to install drivers. Download the Zadig software (version 2.7 or later) from [zadig.akeo.ie](http://zadig.akeo.ie). (You do not need to install it; simply run the downloaded executable.)

To install the driver:

1. Connect the board to your computer with the appropriate cable and power it up.
2. Run the Zadig software.
3. Choose **Options > List All Devices**.
4. Select **Topaz Tz170 J484 Development Kit (Interface 1)**.



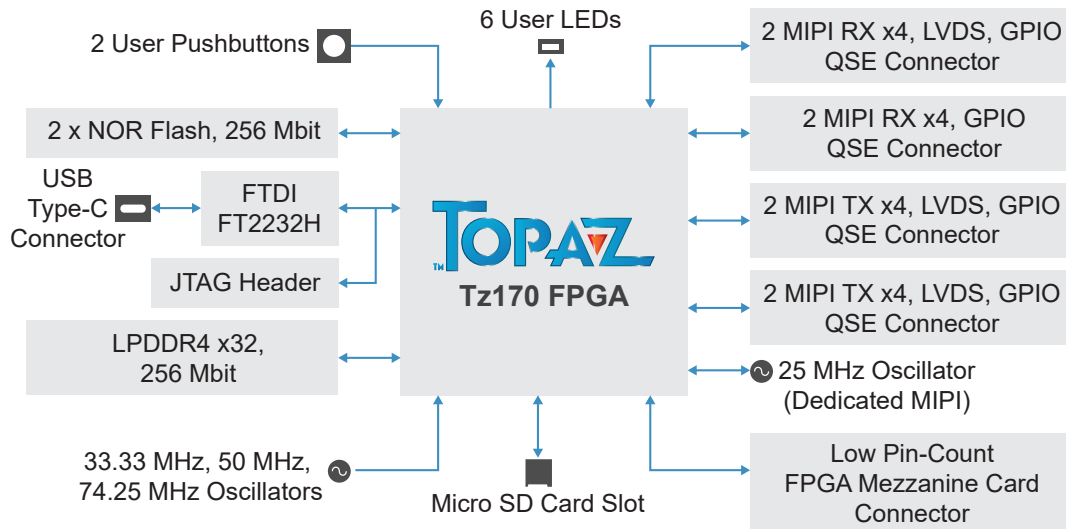
**Note:** You are required to use the default driver for Interface 0 when you connect the Topaz Tz170 J484 Development Board (which uses UART interface) to your computer.

5. Select **libusb-win32** in the **Driver** drop-down list.
6. Click **Replace Driver**.
7. Close the Zadig software.

# Board Functional Description

The Topaz Tz170 J484 Development Board contains a variety of components to help you build designs for the Topaz Tz170 FPGA.

Figure 1: Topaz Tz170 J484 Development Board Block Diagram



## Features

- Efinix Tz170J484I3<sup>(1)</sup> FPGA in a 484-ball FineLine BGA package
- LPDDR4 256 Mbit x32 bits memory, with up to 1.6 Gbps double-data rate.
- 2 x 256 Mbit SPI NOR flash memories
- 4 x MIPI, LVDS, and GPIO high-speed QSE connectors to attach your custom daughter cards
- Micro-SD card slot
- Low pin-count connector (LPC) with user provided FPGA mezzanine card (FMC)
- USB Type-C connector to configure the development board
- 33.33, 50, and 74.25 MHz oscillators for Tz170 PLL input
- User LEDs and switches:
  - 6 LEDs
  - 2 pushbutton switches
- Power:
  - 12.0 V power supply connector
  - On-board regulator sources: 0.62 V, 0.85 V, 0.95 V, 1.1 V, 1.2 V, 1.8 V, 3.3 V, 5.0 V
- Power good and Topaz Tz170 J484 Development Board configuration done LEDs

<sup>(1)</sup> The FPGA speed grade may vary and is subject to availability.

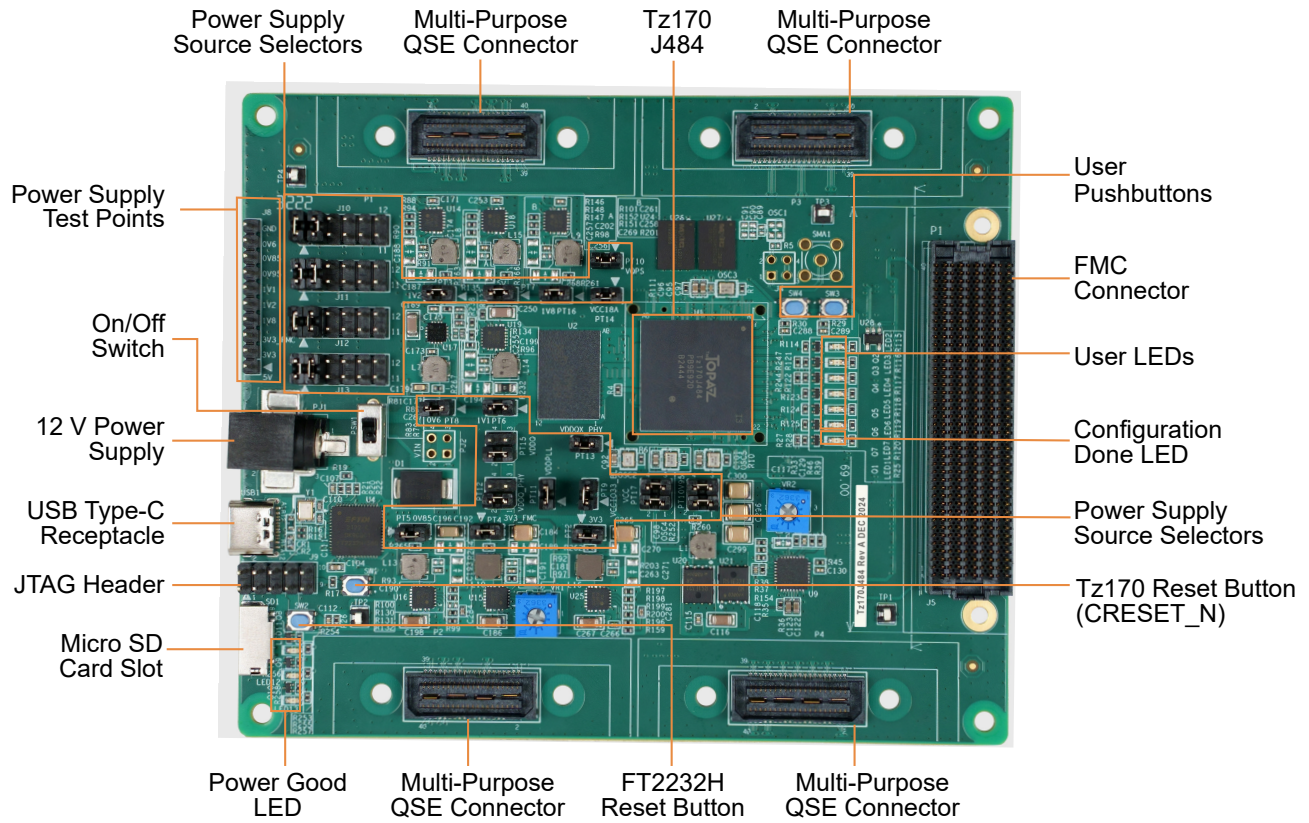
## Overview

The board features the Efnix Tz170 FPGA in a 484-ball FBGA package, which is fabricated using Efnix Quantum<sup>®</sup> technology. The Quantum<sup>®</sup>-accelerated programmable logic and routing fabric is wrapped with an I/O interface in a small footprint package. Tz170 FPGAs also include embedded memory blocks and DSP blocks. You create designs for the Tz170 FPGA in the Efinity<sup>®</sup> software, and then download the resulting configuration bitstream to the board using the USB connection.



**Learn more:** For more information on Tz170 FPGAs, refer to the [Tz170 Data Sheet](#).

Figure 2: Topaz Tz170 J484 Development Board Components (Top)



The Topaz Tz170 J484 Development Board provides four multi-purpose 0.8 mm high-speed ground plane sockets. These sockets can be used for GPIO, MIPI CSI-2 TX/RX, and LVDS TX/RX. The board includes a USB type-C port for the FTDI interface.

The FTDI FT2232H module has two channels to support the following interfaces:

- *FTDI interface 0*—FPGA UART
- *FTDI interface 1*—FPGA JTAG and SPI

The FTDI module receives the Topaz Tz170 J484 Development Board configuration bitstream from a USB host and writes to the Tz170 FPGA in SPI active configuration. You can write a configuration bitstream to the on-board SPI NOR flash memory through JTAG with the [JTAG SPI Flash Loader Core](#). Additionally, it supports a UART interface to the Tz170.

The SPI NOR flash memory stores the configuration bitstream. The Tz170 FPGA accesses this configuration bitstream when it is in active configuration mode (default).



**Learn more:** Refer to the [Topaz Tz170 J484 Development Board Schematics and BOM](#) for more information about the components used.

## Power On

To turn on the development board, turn on switch PSW1. The 12 V DC power is input to the on-board regulators to generate the required 5.0 V, 3.3 V, 1.8 V, 1.2 V, 1.1 V, 0.95 V, 0.85 V, and 0.62 V for components on the board. When these voltages are up and stable, the power-good LEDs, LED11, LED12, and LED13 illuminate, giving you a visual confirmation of the status.

## Reset

The Tz170 FPGA is typically brought out of reset with the `CRESET_N` signal. Upon power up, the Tz170FPGA is held in reset until `CRESET_N` toggles high-low-high.



**Note:** You can manually assert the high-low-high transition with pushbutton switch SW1.

`CRESET_N` has a pull-up resistor. When you press SW1, the board drives `CRESET_N` low; when you release SW1, the board drives `CRESET_N` high. Thus, a single press of SW1 provides the required high-low-high transition.

After toggling `CRESET_N`, the Tz170FPGA goes into configuration mode and reads the configuration bitstream from the flash memory. When configuration completes successfully, the FPGA drives the `CDONE` signal high. `CDONE` is connected to a LED (LED1), which turns on when the Tz170 FPGA enters user mode.

### FTDI Reset

Pushbutton SW2 is the FTDI FT2232H chip reset button. All board communications through the FTDI FT2232H chip disconnect when you press pushbutton SW2, and reconnect when you release it.

## Configuration



**Note:** You need to use Efinity software version 2024.2 patch 3 or higher.

You can configure the Tz170 FPGA using the following configuration modes:

- JTAG
- SPI Active (up to x8) via JTAG Bridge

You can use the JTAG bridge mode when programming the flash. See [Programming the Development Board](#) for SPI Active mode programming operations. You must use the JTAG Bridge when programming the flash because the SPI active signals are not routed directly to FT4232H on the Topaz Tz170 J484 Development Board. When generating bitstreams for your own design, ensure that you select the **Active** option in the **Bitstream Generation** tab of the Efinity **Project Editor**. Refer to [Programming the Development Board](#) for instructions on using SPI active mode.

The Topaz Tz170 J484 Development Board does not support internal reconfiguration for remote updates.



**Note:** For more details on the JTAG SPI bridge loader, refer to [Efinity Software User Guide](#).

## Clock Sources

Three on-board oscillators (33.33, 50, and 74.25 MHz) are available to drive the Tz170 PLL input pin and clock input. Additionally, there is a dedicated 25 MHz on-board oscillator as the MIPI clock source.

*Table 1: Oscillator and Clock Generator Sources*

Clock Source	Tz170 Pin Name	PLL Resource
33.33 MHz oscillator	GPIOL_32_PLLIN1	PLL_TL2
50 MHz oscillator	GPIOB_P_11_PLLIN0	PLL_BL1
74.25 MHz oscillator	GPIOL_26_PLLIN1	PLL_TL0
25 MHz oscillator	GPIOL_06_CLK27_P	MIPI0 dedicated PLL
	GPIOL_07	MIPI1 dedicated PLL
	GPIOL_27_CLK28_P	MIPI2 dedicated PLL
	GPIOL_28_CLK29_P	MIPI3 dedicated PLL



**Note:** The Efinity Interface Designer issues an unrouted clkmux input error if more than 8 GCLK resources are used on the left side of Tz170 FPGA. To solve this, assign one of the clocks, for example MIPI clock TX0, to use the RCLK instead of the GCLK. For more information, refer to the Clock and Control Network section of the [Tz170 Data Sheet](#).

## Headers

The board contains a variety of headers to provide power, inputs, and outputs, and to communicate with external devices or boards.

**Table 2: Topaz Tz170 J484 Development Board Headers**

Reference Designator	Description
P1	40-pin multi-purpose high-speed QSE connector for MIPI TX/RX, LVDS, or GPIO
P2	40-pin multi-purpose high-speed QSE connector for MIPI TX/RX, or GPIO
P3	40-pin multi-purpose high-speed QSE connector for MIPI TX/RX, LVDS, or GPIO
P4	40-pin multi-purpose high-speed QSE connector for MIPI TX/RX, LVDS, or GPIO
PJ1	12 V DC power supply input jack
PT1	0.95 V adjustable power supply source selector
PT2	3.3 V power supply source selector
PT3	1.2 V power supply source selector
PT4	VCCIO and 3.3 V (3V3_FMC) adjustable power supply source selector
PT5	0.85 V power supply source selector
PT6	1.1 V power supply source selector
PT7	5 V power supply source selector
PT8	0.62 V power supply source selector
PT9	VCCIO33 selector for banks BL, BR, TL, and TR (3.3 V)
PT10	VQPS selector (1.8 V)
PT11	VDDPLL/VDD_PHY selector (0.85 V)
PT12	User selectable VDDQ_PHY (0.62 V or 1.1 V)
PT13	VDDQX_PHY selector (1.1 V)
PT14	MIPI selector (1.8 V)
PT15	User selectable VDDQ (0.62 V or 1.1 V)
PT16	1.8 V power supply source selector
PT17	VCCA selector (0.95 V)
J5	FMC connector
J8	Power supply test point
J9	JTAG header
J10	User selectable VCCIO for bank 2A_2B_2C (1.2 V, 1.5 V, or 1.8 V)
J11	User selectable VCCIO for bank 3B_3C (1.2 V, 1.5 V, or 1.8 V)
J12	User selectable VCCIO for bank 3A (1.2 V, 1.5 V, or 1.8 V)
J13	User selectable VCCIO for bank 4A (1.2 V, 1.5 V, or 1.8 V)
USB1	USB type-C receptacle (FTDI FT2232H)
TP1 - TP4	Ground test points
SD1	Micro-SD card slot

## Headers P1, P2, P3, and P4 (Multi-Purpose)

P1, P2, P3, and P4 are multi-purpose high-speed QSE interface connectors for either MIPI TX/RX, LVDS, or GPIO that support 2 clock lanes and 8 data lanes.

**Table 3: P1 Pin Assignments**

Pin Number	Signal Name	Pin Number	Signal Name
1	3V3	2	MIPI1_RXDP0
3	5V	4	MIPI1_RXDN0
5	GND	6	GND
7	MIPI0_RXDP0	8	MIPI1_RXDP1
9	MIPI0_RXDN0	10	MIPI1_RXDN1
11	GND	12	GND
13	MIPI0_RXDP1	14	MIPI1_RXDP2
15	MIPI0_RXDN1	16	MIPI1_RXDN2
17	GND	18	GND
19	MIPI0_RXDP2	20	MIPI1_RXDP3
21	MIPI0_RXDN2	22	MIPI1_RXDN3
23	GND	24	GND
25	MIPI0_RXDP3	26	MIPI1_RXDP4
27	MIPI0_RXDN3	28	MIPI1_RXDN4
29	GND	30	GND
31	MIPI0_RXDP4	32	GPIOL_29_CLK30_P
33	MIPI0_RXDN4	34	GPIOL_03_CLK24_P
35	GND	36	GND
37	GPIOR_66	38	QSE_GPIOT_P_14_CLK17_P
39	GPIOR_65	40	QSE_GPIOT_N_14_CLK17_N

**Table 4: P2 Pin Assignments**

Pin Number	Signal Name	Pin Number	Signal Name
1	3V3	2	MIPI3_RXDP0
3	5V	4	MIPI3_RXDN0
5	GND	6	GND
7	MIPI2_RXDP0	8	MIPI3_RXDP1
9	MIPI2_RXDN0	10	MIPI3_RXDN1
11	GND	12	GND
13	MIPI2_RXDP1	14	MIPI3_RXDP2
15	MIPI2_RXDN1	16	MIPI3_RXDN2
17	GND	18	GND
19	MIPI2_RXDP2	20	MIPI3_RXDP3
21	MIPI2_RXDN2	22	MIPI3_RXDN3
23	GND	24	GND
25	MIPI2_RXDP3	26	MIPI3_RXDP4
27	MIPI2_RXDN3	28	MIPI3_RXDN4
29	GND	30	GND
31	MIPI2_RXDP4	32	GPIOL_04_CLK25_P
33	MIPI2_RXDN4	34	GPIOL_05_CLK26_P
35	GND	36	GND
37	GPIOR_69	38	GPIOB_P_01_EXTFB
39	GPIOR_70	40	GPIOB_P_00_PLLIN0

**Table 5: P3 Pin Assignments**

Pin Number	Signal Name	Pin Number	Signal Name
1	3V3	2	MIPI1_TXDP0
3	5V	4	MIPI1_TXDN0
5	GND	6	GND
7	MIPI0_TXDP0	8	MIPI1_TXDP1
9	MIPI0_TXDN0	10	MIPI1_TXDN1
11	GND	12	GND
13	MIPI0_TXDP1	14	MIPI1_TXDP2
15	MIPI0_TXDN1	16	MIPI1_TXDN2
17	GND	18	GND
19	MIPI0_TXDP2	20	MIPI1_TXDP3
21	MIPI0_TXDN2	22	MIPI1_TXDN3
23	GND	24	GND
25	MIPI0_TXDP3	26	MIPI1_TXDP4
27	MIPI0_TXDN3	28	MIPI1_TXDN4
29	GND	30	GND
31	MIPI0_TXDP4	32	QSE_GPIOT_P_15_CLK18_P
33	MIPI0_TXDN4	34	QSE_GPIOT_N_15_CLK18_N
35	GND	36	GND
37	QSE_GPIOT_P_16_CLK19_P	38	QSE_GPIOT_P_17_CLK20_P
39	QSE_GPIOT_N_16_CLK19_N	40	QSE_GPIOT_N_17_CLK20_N

**Table 6: P4 Pin Assignments**

Pin Number	Signal Name	Pin Number	Signal Name
1	3V3	2	MIPI3_TXDP0
3	5V	4	MIPI3_TXDN0
5	GND	6	GND
7	MIPI2_TXDP0	8	MIPI3_TXDP1
9	MIPI2_TXDN0	10	MIPI3_TXDN1
11	GND	12	GND
13	MIPI2_TXDP1	14	MIPI3_TXDP2
15	MIPI2_TXDN1	16	MIPI3_TXDN2
17	GND	18	GND
19	MIPI2_TXDP2	20	MIPI3_TXDP3
21	MIPI2_TXDN2	22	MIPI3_TXDN3
23	GND	24	GND
25	MIPI2_TXDP3	26	MIPI3_TXDP4
27	MIPI2_TXDN3	28	MIPI3_TXDN4
29	GND	30	GND
31	MIPI2_TXDP4	32	QSE_GPIOT_P_18_CLK21_P
33	MIPI2_TXDN4	34	QSE_GPIOT_N_18_CLK21_N
35	GND	36	GND
37	QSE_GPIOB_P_21_CDI9	38	QSE_GPIOB_P_18_CLK5_P
39	QSE_GPIOB_N_21_CDI8	40	QSE_GPIOB_N_18_CLK5_N

### *Header PJ1 (Power Supply)*

PJ1 is a 12V DC power supply input jack. PJ1 supplies power to regulators on the board that power the Tz170. The maximum current supply to this input jack is 5 A.

## Header J5 (FMC)

J5 is a 400-pin FMC LPC interface connector for connecting the user provided FMC-to-QSE Adapter Card.



**Note:** Only sub-headers J5-1, J5-2, and J5-3 are connected to I/O pins in the Tz170. Sub-headers J5-4 and J5-4 are not connected to any I/O pins in the Tz170



**Important:** The FMC interface on the Topaz Tz170 J484 Development Board does not have JTAG compatibility. Therefore, ensure there is no connection between TDI and TDO on the FMC daughter card because it will interrupt the JTAG access on the Topaz Tz170 J484 Development Board.

**Table 7: Supported Daughter Cards**

The following are daughter cards that can be used on the FMC-to-QSE Adapter Card attached to the FMC interface.

Daughter Card	QSE Interface on the FMC-to-QSE Adapter Card		
	J1	J2	J3
Coral Camera Connector Daughter Card		✓	
Raspberry Pi Camera Connector Daughter Card		✓	
Dual Raspberry Pi Camera Connector Daughter Card		✓	
IMX477 Camera Connector Daughter Card		✓	
Ethernet Connector Daughter Card	✓	✓	
HDMI Connector Daughter Card	✓	✓	
Dual MIPI to DSI Converter Daughter Card	✓	✓	
MIPI and LVDS Expansion Daughter Card	✓	✓	✓

**Table 8: J5-1 Pin Assignments**

Pin Number	Signal Name	Pin Number	Signal Name
C1	GND	D1	GND
C2	N.C.	D2	GND
C3	N.C.	D3	GND
C4	GND	D4	N.C.
C5	GND	D5	N.C.
C6	N.C.	D6	GND
C7	N.C.	D7	GND
C8	GND	D8	GPIOR_P_31_PLLIN1
C9	GND	D9	GPIOR_N_31
C10	GPIOR_P_22_CLK13_P	D10	GND
C11	GPIOR_N_22_CLK13_N	D11	GPIOR_P_27_CLK8_P
C12	GND	D12	GPIOR_N_27_CLK8_N
C13	GND	D13	GND
C14	GPIOR_P_20_CLK15_P	D14	GPIOR_P_25_CLK10_P

Pin Number	Signal Name	Pin Number	Signal Name
C15	GPIOR_N_20_CLK15_N	D15	GPIOR_N_25_CLK10_N
C16	GND	D16	GND
C17	GND	D17	GPIOB_P_16_EXTSPICLK_CLK3_P
C18	GPIOR_P_18	D18	GPIOB_N_16_CLK3_N
C19	GPIOR_N_18	D19	GND
C20	GND	D20	GPIOR_P_45_PLLIN0
C21	GND	D21	GPIOR_N_45
C22	GPIOB_P_23_PLLIN0	D22	GND
C23	GPIOB_N_23_CDI12	D23	GPIOR_P_42
C24	GND	D24	GPIOR_N_42
C25	GND	D25	GND
C26	GPIOB_P_24_EXTFB	D26	GPIOB_P_25_CDI15
C27	GPIOB_N_24_CDI13	D27	GPIOB_N_25_CDI14
C28	GND	D28	GND
C29	GND	D29	TCK
C30	GPIOL_00_PLLIN1	D30	FMC_TDI
C31	GPIOL_36_PLLIN1	D31	FMC_TDO
C32	GND	D32	3V3
C33	GND	D33	FMC_TMS
C34	N.C.	D34	N.C.
C35	12 V	D35	N.C.
C36	GND	D36	3V3
C37	12 V	D37	GND
C38	GND	D38	3V3
C39	3V3	D39	GND
C40	GND	D40	3V3

Table 9: J5-2 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
E1	GND	F1	N.C.
E2	FMC_GPIOT_P_14_CLK17_P	F2	GND
E3	FMC_GPIOT_N_14_CLK17_N	F3	GND
E4	GND	F4	N.C.
E5	GND	F5	N.C.
E6	FMC_GPIOT_P_15_CLK18_P	F6	GND
E7	FMC_GPIOT_N_15_CLK18_N	F7	N.C.
E8	GND	F8	N.C.
E9	FMC_GPIOT_P_16_CLK19_P	F9	GND

Pin Number	Signal Name	Pin Number	Signal Name
E10	FMC_GPIOT_N_16_CLK19_N	F10	N.C.
E11	GND	F11	N.C.
E12	FMC_GPIOT_P_17_CLK20_P	F12	GND
E13	FMC_GPIOT_N_17_CLK20_N	F13	N.C.
E14	GND	F14	N.C.
E15	FMC_GPIOT_P_18_CLK21_P	F15	GND
E16	FMC_GPIOT_N_18_CLK21_N	F16	N.C.
E17	GND	F17	N.C.
E18	GPIOT_P_19_CLK22_P	F18	GND
E19	GPIOT_N_19_CLK22_N	F19	N.C.
E20	GND	F20	N.C.
E21	GPIOB_P_17_CLK4_P	F21	GND
E22	GPIOB_N_17_CLK4_N	F22	N.C.
E23	GND	F23	N.C.
E24	GPIOB_P_22_CDI11	F24	GND
E25	GPIOB_N_22_CDI10	F25	N.C.
E26	GND	F26	N.C.
E27	FMC_GPIOB_P_21_CDI9	F27	GND
E28	FMC_GPIOB_N_21_CDI8	F28	N.C.
E29	GND	F29	N.C.
E30	FMC_GPIOB_P_20_CDI6_CLK7_P	F30	GND
E31	FMC_GPIOB_N_20_CDI7_CLK7_N	F31	N.C.
E32	GND	F32	N.C.
E33	FMC_GPIOB_P_19_CDI5_CLK6_P	F33	GND
E34	FMC_GPIOB_N_19_CDI4_CLK6_N	F34	N.C.
E35	GND	F35	N.C.
E36	FMC_GPIOB_P_18_CLK5_P	F36	GND
E37	FMC_GPIOB_N_18_CLK5_N	F37	N.C.
E38	GND	F38	GND
E39	3V3_FMC	F39	GND
E40	GND	F40	3V3_FMC

Table 10: J5-3 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
G1	GND	H1	N.C.
G2	GPIOT_P_20_CLK23_P	H2	GND
G3	GPIOT_N_20_CLK23_N	H3	GND
G4	GND	H4	GPIOT_P_13_CLK16_P

Pin Number	Signal Name	Pin Number	Signal Name
G5	GND	H5	GPIOT_N_13_CLK16_N
G6	GPIOR_P_16_PLLIN1	H6	GND
G7	GPIOR_N_16	H7	GPIOR_P_24_CLK11_P
G8	GND	H8	GPIOR_N_24_CLK11_N
G9	GPIOR_P_28	H9	GND
G10	GPIOR_N_28	H10	GPIOR_P_23_CLK12_P
G11	GND	H11	GPIOR_N_23_CLK12_N
G12	GPIOR_P_21_CLK14_P	H12	GND
G13	GPIOR_N_21_CLK14_N	H13	GPIOR_P_26_CLK9_P
G14	GND	H14	GPIOR_N_26_CLK9_N
G15	GPIOR_P_19	H15	GND
G16	GPIOR_N_19	H16	GPIOT_P_12_EXTFB
G17	GND	H17	GPIOT_N_12
G18	GPIOR_P_17	H18	GND
G19	GPIOR_N_17	H19	GPIOB_P_15_CLK2_P
G20	GND	H20	GPIOB_N_15_CLK2_N
G21	GPIOB_P_28_CDI21	H21	GND
G22	GPIOB_N_28_CDI20	H22	GPIOR_P_44_EXTFB
G23	GND	H23	GPIOR_N_44
G24	GPIOB_P_27_CDI19	H24	GND
G25	GPIOB_N_27_CDI19	H25	GPIOR_P_43
G26	GND	H26	GPIOR_N_43
G27	GPIOR_P_41	H27	GND
G28	GPIOR_N_41	H28	GPIOB_P_26_CDI16
G29	GND	H29	GPIOB_N_26_CDI17
G30	GPIOB_P_34	H30	GND
G31	GPIOB_N_34	H31	GPIOB_P_33_CDI31
G32	GND	H32	GPIOB_N_33_CDI30
G33	GPIOB_P_32_CDI28	H33	GND
G34	GPIOB_N_32_CDI29	H34	GPIOB_P_31_CDI27
G35	GND	H35	GPIOB_N_31_CDI26
G36	GPIOB_P_30_CDI25	H36	GND
G37	GPIOB_N_30_CDI24	H37	GPIOB_P_29_CDI22
G38	GND	H38	GPIOB_N_29_CDI23
G39	3V3_FMC	H39	GND
G40	GND	H40	3V3_FMC

## Headers PT1, PT2, PT3, PT4, PT5, PT6, PT7, PT8, and PT16 (Power Supply Source Selector)

PT1, PT2, PT3, PT4, PT5, PT6, PT7, PT8, and PT16 are 2-pin or 4-pin (PT1 only) headers reserved to ease power measurements. Refer to the [Topaz Tz170 J484 Development Board Schematics](#) for more information.

By default, the jumpers connect pins 1 and 2 (and 3 and 4 for PT1), which sources the power from on-board regulators.

**Table 11: PT1, PT2, PT3, PT4, PT5, PT6, PT7, PT8, and PT16 (Power Supply Source Selector)**

Header	Description
PT1	0.95 V power supply source selector (adjustable with VR2 potentiometer)
PT2	3.3 V power supply source selector
PT3	1.2 V power supply source selector
PT4	3.3 V (3V3_FMC) power supply source selector (adjustable with VR1 potentiometer)
PT5	0.85 V power supply source selector
PT6	1.1 V power supply source selector
PT7	5 V power supply source selector
PT8	0.62 V power supply source selector
PT16	1.8 V power supply source selector

## Headers PT9, PT10, PT11, PT13, PT14, and PT17 (Functional Power Supply Selector)

PT9, PT10, PT11, PT13, PT14, and PT17 are 2-pin or 4-pin (PT17 only) headers used to select whether to source a power supply from the on-board regulator or an external supply. Each header connects to different functions.

By default, the jumpers connect pins 1 and 2 (and 3 and 4 for PT17), which sources the power from on-board regulators. You can disconnect the jumper and connect an external supply to pin 2.



**Important:** You must remove the jumper at PT10 before powering up the development board.

**Table 12: PT9, PT10, PT11, PT13, PT14, and PT17 (Functional Power Supply Selector)**

Header	Description
PT9	VCCIO33 selector for banks BL, BR, TL and TR (3.3 V)
PT10	VQPS selector (1.8 V)
PT11	VDDPLL/VDD_PHY selector (0.85 V)
PT13	VDDQX_PHY selector (1.1 V)
PT14	MIPI selector (1.8 V)
PT17	VCCA selector (0.95 V)

## Headers PT12 and PT15 (VDDQ\_PHY and VDDQ Selector)

PT12 and PT15 are 4-pin headers used to select the voltage supplies for VDDQ\_PHY and VDDQ. Select these voltage supplies based on the DDR mode you use. By default, the jumper connects pin 3 and 4. You can disconnect the jumpers, and connect an external source to pins 2 and 4.

**Table 13: PT12 and PT15 Pin Assignments**

Jumper	VDDQ_PHY and VDDQ Voltage	DDR Mode
Connect Pins 3 and 4	1.1 V	LPDDR4

## Header J8 (Supply Test Points)

J8 is a 10-pin header connected to the available Topaz Tz170 J484 Development Board power supplies. Connect to the following pins to evaluate the corresponding power supply.

**Table 14: J8 Pin Assignments**

Pin Number	Voltage
1	5 V
2	3.3 V
3	3.3 V (3V3_FMC)
4	1.8 V
5	1.2 V
6	1.1 V
7	0.95 V
8	0.85 V
9	0.62 V
10	GND

## Header J9 (JTAG)

J9 is a 10-pin JTAG interface. You can access the Tz170 JTAG pins through this header.

**Table 15: J9 Pin Assignments**

Pin Number	Signal Name
1	TDO
2	3.3 V
3	TCK
4	TDI
5	TMS
6 <sup>(2)</sup>	FTDI_RST
7	N.C.
8	CRESET_N
9	GND
10	GND

## Headers J10, J11, J12, and J13 (Bank VCCIO Selector)

J10, J11, J12, and J13 are 12-pin headers used to select the VCCIO supply for banks 2A, 2B, 2C, 3A, 3B, 3C, and 4A. By default, the jumpers connect pins 1 and 2, and pins 3 and 4 which is 1.8 V. Connect the jumpers as shown in the following table to change the voltages.

**Table 16: J10, J11, J12, and J13 Pin Assignments**

Jumper	Header			
	J10 Banks 2A, 2B, 2C	J11 Bank 3B_3C	J12 Bank 3A	J13 Banks 4A
Connect Pins 1 and 2	1.8 V (default)			
Connect Pins 3 and 4				
Connect Pins 5 and 6	1.2 V			
Connect Pins 7 and 8				
Connect Pins 9 and 10	3.3 V (3V3_FMC) Set 3V3_FMC to 1.5 V using the VR1 potentiometer <b>before</b> connecting the jumpers.			
Connect Pins 11 and 12				



**Important:** The default voltage out-of-box is 3.3V. If FMC\_VADJ is required, ensure the voltage matches the specifications of your daughter card (e.g., 1.2V, 1.5V, 1.8V, etc.). Additionally, install R140, R141, R142, and R143 with 0R (or shorting) to connect the voltage domain with the FMC connector.

<sup>(2)</sup> This pin will also need to be connected to GND to disable the FTDI chip so the external cable can function.

## Header USB1 (USB FTDI FT2232H)

USB1, a type-C USB receptacle, is the interface between the board and your computer for communication through the FTDI FT2232H chip. Connect the type-C USB cable for configuring the Tz170 FPGA and NOR flash. The board supports three different configuration modes: SPI passive mode, SPI active mode, and JTAG mode.

## Test Points TP1, TP2, TP3, and TP4 (Ground)

Test points TP1, TP2, TP3, and TP4 are test points connected to ground. You can use any of the test points to get a ground reference on the Topaz Tz170 J484 Development Board.

## SD1 (Micro-SD Card Slot)

The Topaz Tz170 J484 Development Board includes a micro-SD card slot, SD1. SD1 connects to GPIO pins in bank TR. The micro-SD supports data rate of up-to 25 MBps.

**Table 17: SD1 Pin Assignments**

Pin Name	Signal Name	Tz170 Pin Name
DATA2	SD_DATA2	GPIOR_58
DATA3	SD_DATA3	GPIOR_59
CMD	SD_CMD	GPIOR_60
VDD	3V3	-
CLK	SD_CLK	GPIOR_62
GND	GND	-
DATA0	SD_DATA0	GPIOR_61
DATA1	SD_DATA1	GPIOR_63
GND	GND	-
GND	GND	-

## User Outputs

The board has 6 user LEDs that are connected to I/O pins in Tz170 banks 4B and 4C. By default, the Tz170 I/O connected to these LEDs are set as active high. To turn a given LED on, pull the corresponding I/O signal high.



**Note:** When adding these GPIO in the Efinity® Interface Designer, configure them as output pins.

*Table 18: User Outputs*

Reference Designator	Tz170 Pin Name	Active
LED2	GPIOB_N_02_CSO	High
LED3	GPIOB_P_02_CSI	High
LED4	GPIOB_P_13_CBSEL0_CLK0_P	High
LED5	GPIOB_P_14_NSTATUS_CLK1_P	High
LED6	GPIOB_N_11	High
LED7	GPIOB_P_12_EXTFB	High

## User Inputs

The board has 2 pushbutton switches that you can use as inputs to the Tz170 FPGA. The pushbuttons are connected to I/O pins in Tz170 bank 4B. When building designs using these switches, turn on an internal pull up for these pins in the Interface Designer.

When you press the pushbutton switches the signal drives low, indicating user input.

*Table 19: User Pushbuttons*

Reference Designator	Tz170 Pin Name	Active
SW3	GPIOB_N_13_CBSEL1_CLK0_N	Low
SW4	GPIOB_N_14_TEST_N_CLK1_N	Low

# Installing Standoffs

Before using the board, attach the standoffs with the screws and nuts provided in the kit. The following table lists the standoffs, screws, and nuts required for standoffs installation.



**Note:** Always power off the development board before attaching the standoffs.

*Table 20: Standoffs and Screws for Standoff Installation*

Standoff			Screw		
Size	Length	Qty	Size	Length	Qty
M3	10 mm	4	M3	6 mm	4

*Figure 3: Installing Standoffs*



To install standoffs, attach four 10 mm standoffs to the Topaz Tz170 J484 Development Board with screws.

Once the standoffs are installed securely, you can make the connections to the development board, for example, connecting the USB cable.



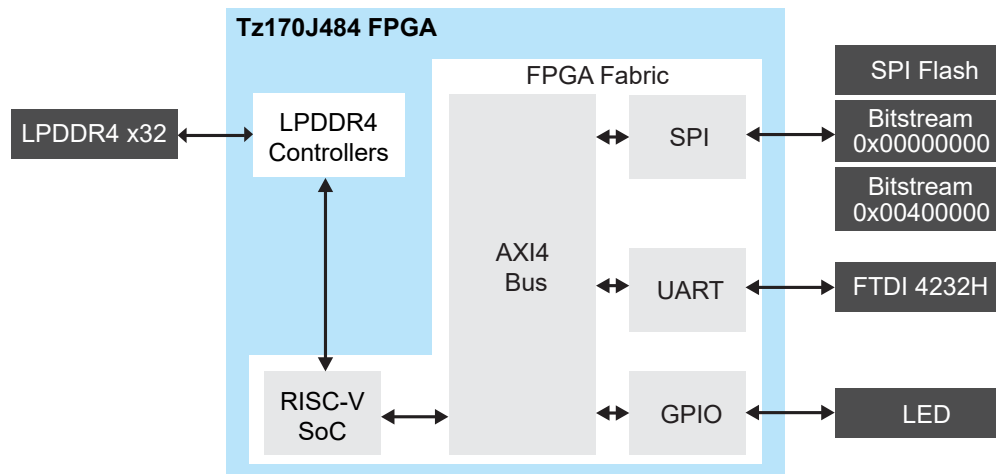
**Warning:** You can damage the board if you over tighten the screws. Tighten all screws to a torque between  $4 \pm 0.5$  kgf/cm and  $5 \pm 0.5$  kgf/cm.

# Topaz Tz170 J484 Development Board Example Design

Efinix preloads the Topaz Tz170 J484 Development Board with an example design that demonstrates the following functions:

- Calculate the moving positions of a spinning donut and render the image through the UART.
- Make an alternate blink on 3 LEDs to show a running light effect by blinking the LEDs in an alternate pattern.

Figure 4: Example Design Block Diagram Overview



## The Spinning Donut Program

This program was invented by Andy Sloane in 2006. It draws a spinning donut in ASCII characters and sends the data through a UART to a PC terminal. Andy Sloane explained the math behind the program to do the 3D rendering and its movement in his article, [Donut math: how donut.c works](#).

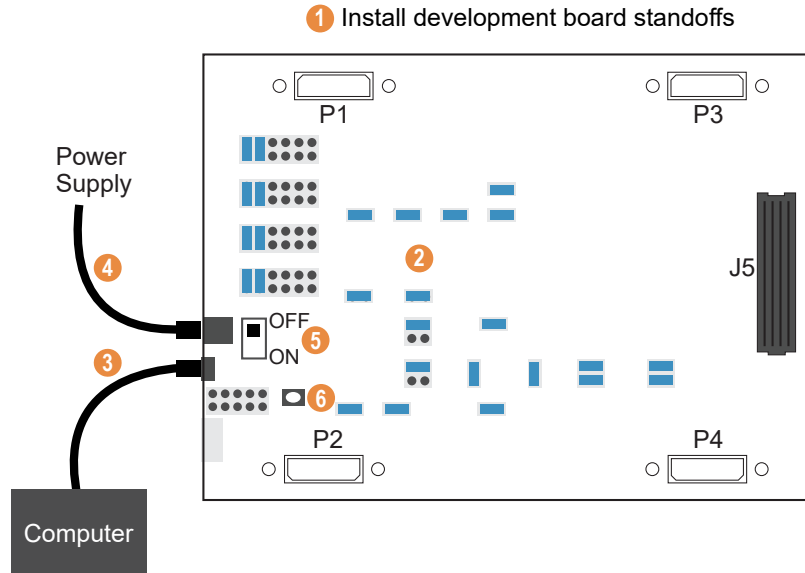
## The Running Light Program

This program demonstrates that the Sapphire RISC-V SoC example design is actively running on the development board. The LEDs light up in series with a short delay between each one.

## Set Up the Hardware

The following figure shows the hardware setup steps:

Figure 5: Hardware Setup



**Important:** Always switch off the power supply and board's power switch before attaching or detaching cables.

1. Install standoffs on the Topaz Tz170 J484 Development Board as described in [Installing Standoffs](#).
2. Ensure that all boards have the following jumper settings:

Board	Header	Pins to Connect
Topaz Tz170 J484 Development Board	J9 and PT10	N.C.
	J10, J11, J12, J13, PT1, and PT17	1 - 2 and 3 - 4
	PT2, PT3, PT4, PT5, PT6, PT7, PT8, PT9, PT11, PT13, PT14, and PT16	1 - 2
	PT12 and PT15	3 - 4

3. Connect the USB header to a USB port of your computer.
4. Ensure the power supply and board power switch (PSW1) are turned off, then connect the 12 V power cable to the board connector and a power source.



**Important:** You must remove the jumper at PT10 before powering up the development board.

5. Turn on the power supply and the board's power switch (PSW1).
6. After turning on the board, press pushbutton SW1 (CRESET\_N).

The board LEDs light up to indicate the following board status.

*Table 21: Board LED Outputs*

<b>LED</b>	<b>Description</b>
LED11, LED12, and LED13 turned on	Power good
LED1 turned on	FPGA configuration done
LED6 turned on	DDR configuration done
LED2 turned on	DDR memory test done
LED3 blinking	Configuration done
LED4 blinking	Configuration done
LED5 blinking	Configuration done



## Creating Your Own Design

The Topaz Tz170 J484 Development Board allows you to create and explore designs for the Tz170 FPGA. Efinix® provides example code and designs to help you get started:

- Our Support Center ([www.efinixinc.com/support](http://www.efinixinc.com/support)) includes examples targeting the board.
- The Efinity® software includes also example designs that you can use as a starting point for your own project and includes a step-by-step tutorial.

## Restoring the Demonstration Design

After you have used the board for other designs, you may want to go back to the original pre-loaded example design.



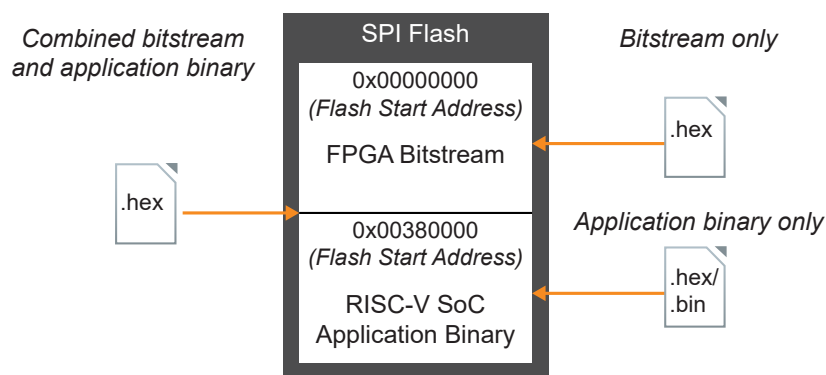
**Note:** The preloaded example design project file is available in the [Topaz Tz170 J484 Development Board Demonstration Design](#) page. The example design page includes the required Efinity software version to compile the design.

The example design consists of the FPGA bitstream and the RISC-V SoC application binary. You need to program these files if you want to restore the example design. There are two ways of programming the files into the SPI flash:

- Program the FPGA bitstream and the application binary together with a combined bitstream
- Program the FPGA bitstream and the application binary separately with two bitstreams

Generally, you use the combined bitstream to quickly restore the entire example design. Use the separate bitstream if you want to restore either the FPGA bitstream or the application binary portion only.

*Figure 7: Example Design SPI Flash Content*



## Example Design Files

The example design includes the following design files.

*Table 22: Design Example File and Directories*

File or Directory	Description
TZ170J484_DK\TZ170J484_DK.xml	Example design project file.
TZ170J484_DK\Bitstream\RestoreBitstream\combine_TZ170J484_oob.hex	Combined file consists of the FPGA bitstream and RISC-V SoC application binary. Program this file into the SPI flash using SPI active configuration mode.
TZ170J484_DK\Bitstream\RestoreBitstream\FPGA_TZ170J484_oob.hex	FPGA bitstream only. Program this file into the SPI flash using SPI active configuration mode.
TZ170J484_DK\Bitstream\RestoreBitstream\FW_TZ170J484_oob.hex	RISC-V SoC application binary only. Program this file into the SPI flash using SPI active configuration mode.
TZ170J484_DK\Bitstream\RestoreBitstream\FPGA_TZ170J484_oob.bit	FPGA bitstream only. Use this file to configure the Tz170 FPGA using JTAG mode configuration.
TZ170J484_DK\Bitstream\SocFW\oob.elf	Pre-compiled example design application binary file to run using OpenOCD Debugger.
TZ170J484_DK\Bitstream\SocFW\oob.bin	Pre-compiled example design application binary file to program into SPI flash using OpenOCD Debugger.
TZ170J484_DK\Bitstream\Bootloader\bootloader.hex	Pre-compiled SPI flash bootloader binary file. The example design does not use the default Sapphire RISC-V SoC SPI flash bootloader. Use this bootloader to overwrite the default SPI flash bootloader if you regenerate the Sapphire RISC-V SoC in IP Manager.
TZ170J484_DK\Bitstream\Bootloader\bootloader.elf	Pre-compiled bootloader binary file to run using OpenOCD Debugger.
TZ170J484_DK\embedded_sw\efx_soft_soc	RISC-V SoC workspace. Use the files in <b>efx_soft_soc</b> if you are using the Efinity RISC-V IDE.
TZ170J484_DK\embedded_sw\efx_soft_soc\software\standalone\oob	RISC-V SoC example design project files.
TZ170J484_DK\embedded_sw\efx_soft_soc\software\standalone\bootloader	RISC-V SoC bootloader project files.



**Learn more:** Before working with the RISC-V SoC included with this example design, you should already be familiar with using the Sapphire SoC and Efinity RISC-V Embedded Software IDE. Refer to the [Sapphire RISC-V SoC Hardware and Software User Guide](#) for more information about the Sapphire SoC.

# Programming the Development Board



**Note:** This section describes the steps to program the example design FPGA bitstream and RISC-V SoC application binary using the SPI Active mode in Efinity Programmer with **.hex** and **.bit** files. For instructions to program or boot the RISC-V SoC application binary using the OpenOCD Debugger with **.bin** or **.elf** files, refer to the [Sapphire RISC-V SoC Hardware and Software User Guide](#).

Before programming the board, connect the Topaz Tz170 J484 Development Board to your computer using a USB cable and power-on the board. Refer to [Table 22: Design Example File and Directories](#) on page 29.

## Combined Bitstream

To program the combined bitstream into the SPI flash using SPI Active using JTAG Bridge (New) mode<sup>(3)</sup>:

1. Choose the **USB Target** (i.e., Topaz Tz170 J484 Development Board).
2. Choose the **SPI Active using JTAG Bridge (New)** programming mode.
3. In the **Image** box, click the **Select Image File** button and select **combine\_TZ170J484\_oob.hex**.
4. Turn on the **Auto configure JTAG Bridge Image** option.
5. Ensure that the **Starting Flash Address** is set to **0x00000000**.
6. Click **Start Program** button. The Programmer will configure the FPGA to JTAG Bridge mode and then program the flash device.

## Separate FPGA Bitstream and Application Binary

To program the FPGA bitstream into the SPI flash using JTAG Bridge (New) mode<sup>(3)</sup>:

1. Choose the **USB Target** (i.e., Topaz Tz170 J484 Development Board).
2. Choose the **SPI Active using JTAG Bridge (New)**.
3. In the **Image** box, click the **Select Image File** button and select **FPGA\_TZ170J484\_oob.hex**.
4. Turn on the **Auto configure JTAG Bridge Image** option.
5. Ensure that the **Starting Flash Address** is set to **0x00000000**.
6. Click **Start Program** button. The Programmer will configure the FPGA to JTAG Bridge mode and then program the flash device.

To program the application binary into the SPI flash using JTAG Bridge (New) mode<sup>(3)</sup>:

1. Choose the **USB Target** (i.e., Topaz Tz170 J484 Development Board).
2. Choose the **SPI Active using JTAG Bridge (New)**.
3. In the **Image** box, click the **Select Image File** button and select **FW\_TZ170J484\_oob.hex**.
4. Turn on the **Auto configure JTAG Bridge Image** option.
5. Ensure that the **Starting Flash Address** is set to **0x00380000**.
6. Click **Start Program** button. The Programmer will configure the FPGA to JTAG Bridge mode and then program the flash device.

<sup>(3)</sup> For SPI Active using JTAG Bridge (Legacy) mode, refer to the [Efinity Software User Guide](#).

# Revision History

*Table 23: Revision History*

<b>Date</b>	<b>Version</b>	<b>Description</b>
March 2025	1.1	Added table Supported Daughter Cards and note in FMC header topic. (DOC-2428)
February 2025	1.0	Initial release. (DOC-2139)