Efinix® Trion® FPGA Overview

The Efinix® Trion® programmable platform, built on Efinix Quantum® technology, delivers substantial Power-Performance-Area advantages over traditional FPGA products. Trion FPGAs feature programmable logic and a routing fabric built using Quantum technology. The fabric is wrapped with an I/O interface in a small footprint package that is required by many high-volume applications such as mobile and IoT. In addition to logic and routing, the fabric includes embedded memory blocks and multiplier blocks (or DSP blocks).

Figure 1 Trion FPGA Block Diagram

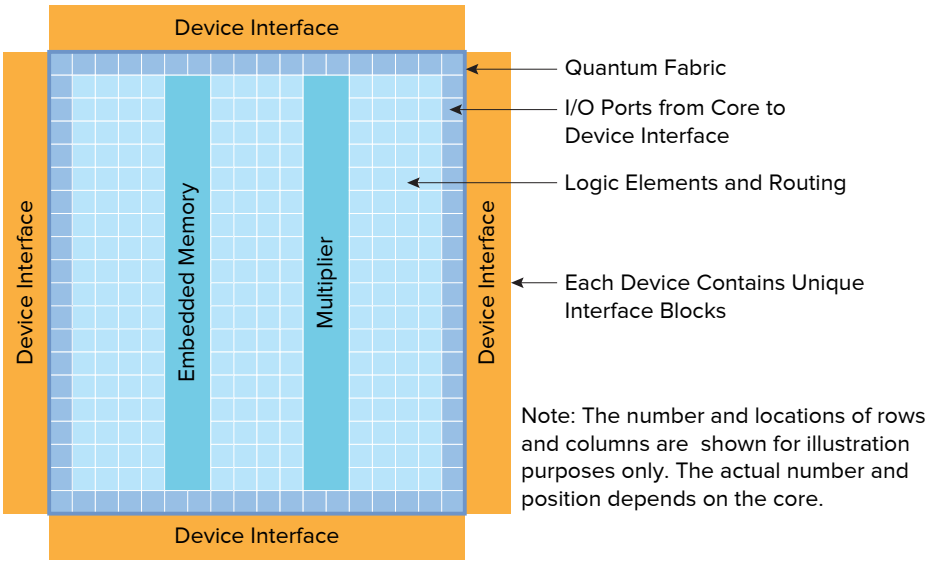

Table 1 Trion Resources and Interfaces

Feature	T4	T8	T13	T20	T35	T55	T85	T120
Logic Elements (LEs)	3,888	7,384	12,828	19,728	31,680	54,195	84,096	112,128
Mask Programmable Memory	√	√	√	√	—	—	—	—
Embedded RAM bits (kb)	77	123	727	1,044	1,475	2,765	4,055	5,407
Embedded 5K RAM blocks	15	24	142	204	288	540	792	1,056
18x18 Multipliers	4	8	24	36	120	150	240	320
PLLs	1	5	5	7	7	8	8	8
LVDS (TX, RX)	—	6, 6	13, 13	20, 26	20, 26	52, 52	52, 52	52, 52
DDR3, LPDDR3, LPDDR2 (up to 1066 Mbps)	—	—	—	x16	x16	x32	x32	x32
MIPI 4-lane DPHY with built-in CSI-2 controller	—	—	2 RX 2 TX	2 RX 2 TX	2 RX 2 TX	3 RX 3 TX	3 RX 3 TX	3 RX 3 TX

The first-generation Trion platform is built on SMIC's 40LL process, with a logic density range from 4K to 120K logic elements (LEs) and standard interfaces such as GPIO, PLLs, oscillators, MIPI, DDR, LVDS, etc.
Trion FPGAs target general-purpose custom logic markets (mobile, IoT, general consumer, industrial, and medical) as well as fast-growing markets such as compute acceleration and deep learning in edge devices.

Standard I/O Interfaces

The initial rollout of Trion FPGAs supports the following interfaces:

- MIPI—4-lane MIPI D-PHY with a built-in (hardened) CSI-2 controller and up to 6 Gbps per PHY. Achieves low power and low cost, and provides a royalty-free, easy implementation for MIPI CSI-2.
- LVDS—Up to 800 Mbps LVDS data rate.
- DDR—Provides DDR3, LPDDR3, LPDDR2 support. Up to 1066 Mbps DDR line rates with up to 51.2 Gbps peak bandwidth. DDR Interface includes hardened PHY and memory controller, providing low power, low cost, and easy to integrate memory interface.

Configuration

T4, T8, T13, and T20 FPGAs offer optional Mask Programmable Memory (MPM). With this feature, you use on-chip MPM instead of an external flash to configure the FPGA. This option is for systems that require an ultra-small form factor and the lowest cost structure such that an external serial flash device is undesirable and/or not required at volume production. MPM is a one-time factory programmable option that requires a Non-Recurring Engineering (NRE) payment. T20 and T13 in LQFP100F3 packages include internal SPI flash that can store multiple configuration bitstreams, non-volatile user data or RISC-V application code for reduced system footprint, power consumption and design complexity.

Efinity Software Support

The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, timing analysis, and debugging. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The software-generated bitstream file configures Trion devices. The software supports the SystemVerilog, Verilog HDL, and VHDL languages.

In Production Now

The Trion FPGAs are in production now. Our development kits and samples are available for purchase on DigiKey and from your local distributor. Visit us online at www.efinixinc.com.

Table 2 Package Options

The MIPI and DDR interfaces have dedicated I/O; therefore; the GPIO number does not include the I/O count for those interfaces.

Package	Pitch (mm)	Size (mm)	GPIO	PLLs	SPI Flash (Mbit)	LVDS Pairs TX, RX	MIPI CSI-2 RX, TX	DDR DRAM	T4	T8	T13	T20	T35	T55	T85	T120
49-ball FBGA	0.4	3x3	33	1					√	√						
80-ball WLCSP	0.4	3.6x4.5	33	3			1, 1					√				
81-ball FBGA	0.5	5x5	55	1					√	√						
100-pin LQFP	0.5	14x14	65	5	16	4, 4					√	√				
144-pin LQFP	0.5	20x20	97	5		6, 6				√		√				
169-ball FBGA	0.65	9x9	73	5		8, 12	2, 2				√	√				
256-ball FBGA	0.8	13x13	195	5		13, 13					√	√				
			191	7		10, 18							√			
324-ball FBGA	0.65	12x12	130	7		20, 26	2, 2	x8, x16				√	√	√	√	√
400-ball FBGA	0.8	16x16	230	7		20, 26		x8, x16				√	√			
484-ball FBGA	0.8	18x18	256	8		40, 40		x16, x32						√	√	√
576-ball FBGA	0.65	16x16	278	8		52, 52	3, 3	x16, x32						√	√	√

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