Titanium SGMII 1G and 2.5G User Guide

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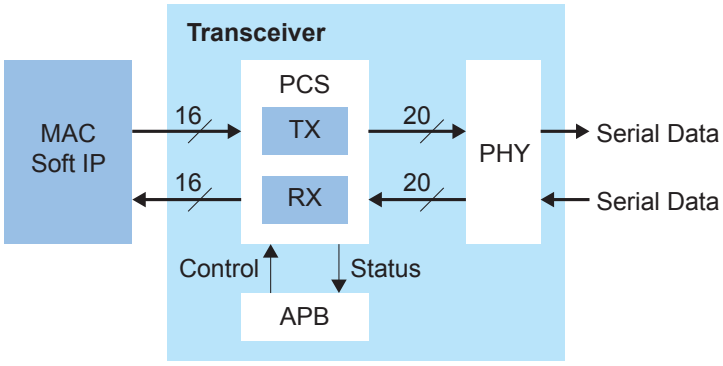
Contents

Introduction

Titanium transceivers consist of a physical medium attachment (PMA) and a physical coding sublayer (PCS). The PMA connects the FPGA to the lane, generates the required clocks, and converts the data from parallel to serial or serial to parallel. The PCS contains the digital processing interface between the PMA and the FPGA fabric. The PCS supports SGMII, 10GBase-KR, and PCIe Gen4 as well as PMA Direct. This user guide provides the specifications for the SGMII interface.

Figure 1: System-Level Block Diagram



Features

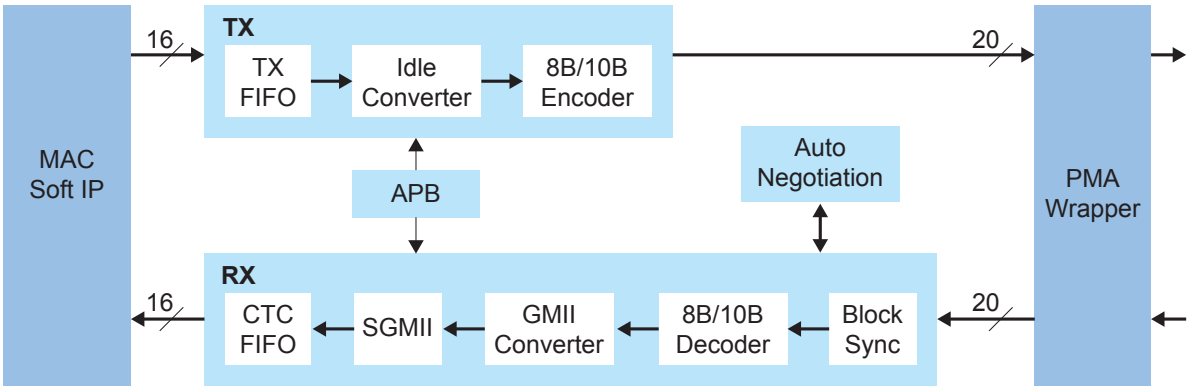
- Per-lane 20b SXGMII interface supports
  - 10 Mbps, 100 Mbps, and 1 Gbps MAC Ethernet data rates for 1G SGMII
  - SerDes rate of 1.25 or 3.125 Gbps
  - Core f_{MAX} of 62.5 or 156.25 MHz
  - Idle conversion
  - 8B/10B encoding/decoding
  - Lane synchronization
  - ±100 ppm clock tolerance
  - Transport of Low Power Idle indicator as described in IEEE P802.3az
  - 16 Kb jumbo packets with minimum inter-packet gap
  - Full duplex
  - SGMII Clause 37 auto-negotiation capability for 1G SGMII
  - Activity status signals for driving external LEDs
- APB control status register interface

Functional Description

The SGMII PCS is a 1G or 2.5G full duplex interface. Each port accepts packet data from the MAC, performs GMII to 8B code group conversion, and performs 8B/10B encoding prior to passing the data to the SerDes module for transmission. The transmit path has an additional data buffer between the MAC and the PCS TX to decouple the PCS from the MAC, simplify clock tree insertion, and provide support 10/100M SGMII operation.

Each port on the receive path takes the unaligned data from the relevant SerDes module, re-aligns each lane to the correct 10B boundary, decodes the data, converts the resulting 8B codewords into GMII traffic, and passes the data through a clock tolerance compensation buffer. This data is then passed to the MAC through a 16-bit GMII interface.

Figure 2: Funtional Block Diagram



CTC: Clock tolerance compensation

Transmitter (TX)

The transmitter comprises a FIFO, SGMII converter, and 8B/10B encoder.

TX FIFO

The Tx FIFO performs these functions:

- Separates the soft MAC clock and the SGMII PCS internal clock. The MAC clock and PCS clock must come from the same clock source with different phase shifts.
- Performs data duplication when the MAC speed is 10 MHz or 100 MHz.

For 10 MHz speeds, the MAC interface runs at 0.625 MHz and each data repeats 100 times. The PCS logic after the TX FIFO consistently runs at 62.5 MHz.

GMII Conversion

This block implements the transmit function as specified in the IEEE Std. 802.3 specification Clause 36.

8B/10B Encoder

The 8B/10B encoder converts 8B data to 10B data and converts any illegal control data into error codes.

Receiver (RX)

The receiver comprises a block synchronizer, 8B/10B encoder, 8B to GMII converter, and clock tolerance compensation FIFO.

Block Synchronizer

The block synchronizer detects the data boundary of the RX recovered SerDes data. It detects the |K| special comma code from the incoming data and aligns the received data to its correct boundary.

8B/10B Decoder

The 8B/10B decoder block decodes the received 10B data to 8B data and replaces any invalid codes with error characters.

GMII Converter

This block implements the receive function as specified in the IEEE Std. 802.3 specification Clause 36. It converts 8B data codes to GMII format.

It also connects to the auto-negotiation state machine to indicate the received code groups type and propagate the configuration code from the link partner.

SGMII Converter

This block generates a data valid strobe before feeding the data to the clock tolerance compensation (CTC) FIFO. In 1G mode, the strobe signal is always active. When operating in 10 Mbps or 100 Mbps mode, this strobe is active once every 50/5 cycles to optimize (remove) the unnecessary repeated data.

CTC FIFO

The CTC FIFO converts the incoming data from the SerDes recovered clock domain to the SGMII PCS clock domain. It inserts or deletes the skip order set within the IPG to compensate for frequency differences between the clock domains up to ±100 ppm.

Auto Negotiation

Each RX lane has its own auto-negotiation state machine as shown in **Figure 2** on page 4. APB interface manages the auto-negotiation function. The auto-negotiation function complies with IEEE Std. 802.3 Clause 37 for next page operation support and can be configured to support link status notifications.

Each port has interrupt pins to allow software notification when auto-negotiation completes or, in the case of a next page operation, to indicate further page data should be written through the APB.

The design should be held in reset as the clock frequency changes.

If you also use auto-negotiation for SGMII operation, the off-chip PHY can use auto-negotiation to exchange link status information. In this case, the link status information

conveys the link state as well as the expected SGMII operating speed. If the speed indicated by the link status does not match the current configured speed, hold the selected port in reset and change the speed mode. On release of reset, the auto-negotiation process automatically restarts and the link status from the off-chip PHY should match the newly configured speed mode.

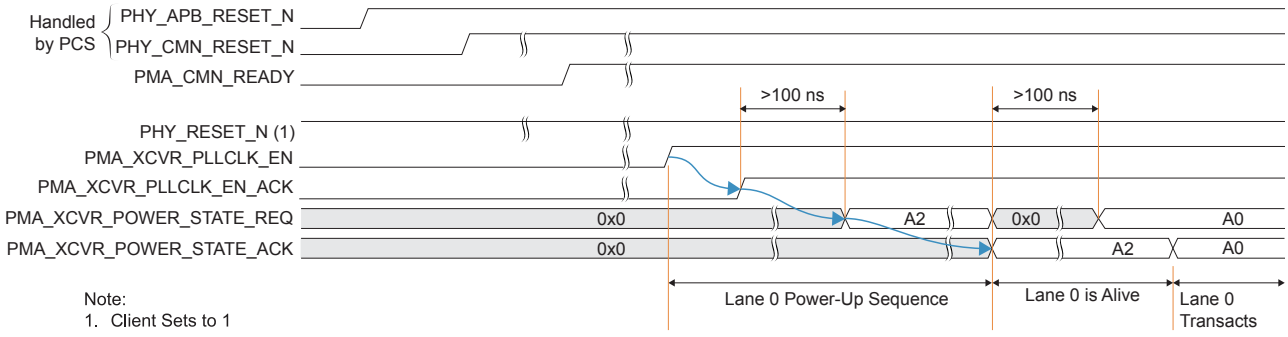
Power-Up Sequence

Initially, the SGMII reset controller controls the `phy_apb_reset_n` and `phy_cmn_reset_n` signals. `phy_cmn_reset_n` is handed over to the user application after the assertion of `pma_cmn_ready` and the FPGA enters user mode. For the power-up sequence to work correctly, the user application must drive the per-lane `phy_reset_n` and `phy_cmn_reset_n` high in it's initial state.

Upon the assertion of `pma_cmn_ready`, `pma_xcvr_power_state_req` is set to 0x0 and `pma_xcvr_pllclk_en` is asserted high. When `pma_xcvr_pllclk_en_ack` goes high, `pma_xcvr_power_state_req` is set to `A2`.

Note: There is a 100 ns (minimum) delay between the assertion of `pma_xcvr_pllclk_en_ack` and the setting of `pma_xcvr_power_state_req` to `A2`.

Figure 3: Power-Up Sequence



signal_ok Assertion Time

To help isolate the receive path during times when the clocking is unreliable, the PCS block implements a `signal_ok` signal such that it resets the whole receiver path, including returning the synchronisation state machine to the LOSS_OF_SYNC state, flushing the CTC buffers, and forcing the alignment state machine to LOSS_OF_ALIGN state. `signal_ok` should be deasserted whenever clocks are unreliable.

The client should program the `signal_ok` register bit high after RX calibration upon the assertion of the PMA signal, `rx_signal_detect`, so that the RX starts operation.

Figure 4: Asserting signal_ok

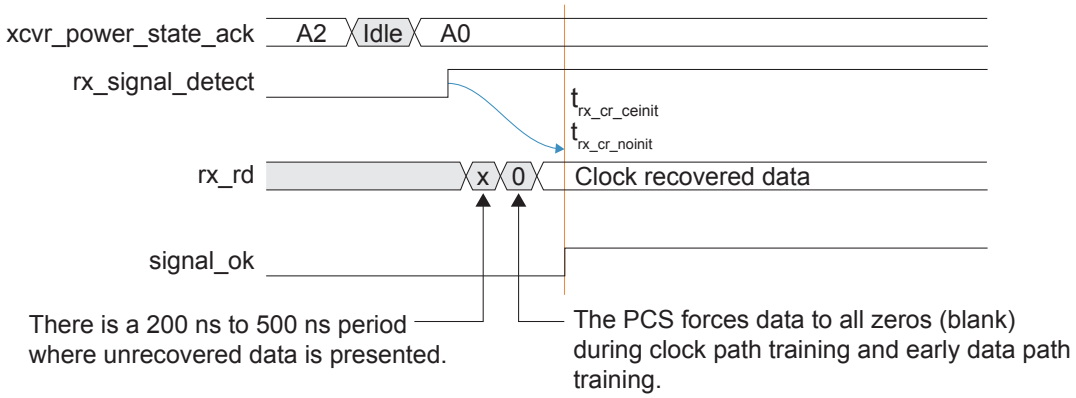


Table 1: signal__ok Timing Parameters

Timing Parameters	Minimum	Maximum	Description
$t_{rx\_cr\_ceinit}$	2,001.613 µs	3,201.806 µs	Initial time required to lock clock recovery once valid data is received.
$t_{rx\_cr\_noinit}$	1,389 ns	1,622 ns	Time required to lock clock recovery once valid data is received, assuming initial adaptation has been previously completed.

To start RX operation, the client monitors the assertion of the PMA `rx_signal_detect` and waits for $t_{rx\_cr\_ceinit}$ or $t_{rx\_cr\_noinit}$ before programming `signal_ok` high.

Auto-Negotiation Mode

The auto-negotiation function can operate in one of two modes: SGMII link state notification and SGMII link state notification with fixed base page

SGMII Link State Notification Mode

When connecting to an SGMII PHY, the PHY uses the same auto-negotiation mechanism to convey link status information to the MAC as defined in the SGMII specification. Although the same state machine is re-used, the transmitted and received configuration code words have different meanings and should be interpreted appropriately.

To enable SGMII link state notification, set up the following registers prior to release of the datapath resets for the affected port:

- **Auto-Negotiation Advertised Abilities**

SGMII CFG1

The `sgmii_an_mode` field should be set to `1`. The `an_link_timeout_val` field should already be set to `0x186a0` to provide the required 1.6 ms timeout value in SGMII mode (16 ns clock period). Therefore, you do not need to set anything else.

Once this mode is set up, the operation is autonomous and you only need to monitor the `pcs_an_complete_*` interrupt pins and take the appropriate action to change the MAC

clock frequencies if the PHY indicates it is operating at a different speed. Note that in such cases, the resets for the affected port should be asserted and only de-asserted once the new clocks are stable.

SGMII Link State Notification (Fixed Base Page) Mode

This mode is the same as the SGMII Link State Notification mode except the Advertised Abilities register does not need to be programmed and the PCS always transmits a Configuration Ordered Set with the code word fixed at `0x4001`. This mode is used for cases where auto-negotiation fails if the link partner is checking for a fixed code word due to differences in interpretation of an ambiguous section of the SGMII specifications.

In addition to the register setup for SGMII Link State Notification mode, set the `alt_sgmii_an_mode` field in the SGMII CFG1 register to 1.

Link Timer Setup

The following register should be setup appropriately for the correct link timer values depending on the desired operating mode. The following registers are used to configure the link timer values:

- **SGMII CFG1**—Set the `an_link_timeout_val` field to provide a 1.6 ms timeout value in SGMII mode or 10 ms in other modes. The default value provides 10 ms assuming a 16 ns clock period for the SerDes recovered clock.
- **SGMII CFG2**—Set the `an_link_fail_timeout_val` field to 10 ms in all modes. This number is the default value for this register assuming a 16 ns clock period for the SerDes recovered clock.

The link timers may be shortened to speed up simulations, however, the correct values must be set up in silicon for interoperability with other devices.

Signals

In the Efinity Interface Designer, signals are prefixed with a user-defined instance name. Efinix recommends using an instance name with the format Q*n*_L*m* (where *n* is the quad number and *m* is the lane number) for easier identification.

Table 2: Signals per Lane

Where *m* is 0, 1, 2, or 3; *x* is a, b, c, d

Signal	Direction	Clock Domain	Description
Clock and Reset			
PCS_CLK_TX	Output	N/A	TX PCS clock source.
PCS_CLK_RX	Output	N/A	RX PCS clock source.
PCS_RST_N_TX	Input	Async	TX PCS reset.
PCS_RST_N_R	Input	Async	RX PCS reset.
PHY_RESET_N	Input	Async	Per lane PMA reset. User needs to initialize to 1.
RX_FWD_CLK	Output	Async	Unused.
TX_FWD_CLK	Output	Async	Forwarded MAC clock from the PCS. PCS_CLK_TX/RX should source from this clock. 10M: 0.625 MHz 100M: 6.25 MHz 1G: 62.5 MHz 2.5G: 156.25 MHz
Control			
PMA_TX_ELEC_IDLE	Input	Async	PMA TX electrical idle. 1: TX lines in an idle state. 0: Transmit data.
Error and Status			
CTC_ERR	Output	PCS_CLK_RX	CTC FIFO error occurred for each CTC module. This signal is clocked by the respective MAC clock for that lane/port. In 10G mode, this signal is rx_clk.
RX_ACTIVITY	Output	PCS_CLK_RX	Optional receive status activity LED output. If configured for 10G support only, this signal is a single output clocked on xcv_0_rbc. If the design is configured for 1G support, this signal is a 4-bit output with each bit corresponding to the respective lane. When operating in 10G mode, only bit 0 toggles.
SYNC_STATUS	Output	PCS_CLK_RX	Comma alignment synchronization status for lane *n*. If operating in GMII mode, each synchronization status is clocked by the respective MAC clock for that lane/port.

Signal	Direction	Clock Domain	Description
TX_ACTIVITY	Output	PCS_CLK_RX	Indicates that the block lock has been achieved either through FEC decoding or the standard RX synchronization process. In addition, if USXGMII auto-negotation is enabled, this output only goes high when auto-negotiation completes.
Power Up			
PMA_RX_SIGNAL_DETECT	Output	Async	PMA receiver signal detect. Asserted high upon detection of the high-speed signal on RX differential inputs.
PMA_XCVR_PLLCLK_EN_ACK	Output	Async	Link PLL clock enable acknowledgment. This signal indicates whether the pma_pllclk_datart_ln_*m* and pma_pllclk_-fullrt_ln_*m* for the associated link/port is running.
PMA_XCVR_PLLCLK_EN	Input	Async	Link PLL clock enable. This signal cleanly gates the pma_pllck_datart_ln_*m* and pma_pllclk_fullrt_ln_*m* clocks for the associated link/port.
PMA_XCVR_POWER_STATE_ ACK[3:0]	Output	Async	Link power state acknowledgment. This signal provides indication that a power state change request has completed. 4'b000000: Value after reset, prior to first power state request. 4'b0001: A0. 4'b0010: A1. 4'b0100: A2. 4'b1000: A3. Once a power state is acknowledged, the value remains unchanged until a new power state is requested and the link has completed the transition to the new power state.
PMA_XCVR_POWER_STATE_ REQ[3:0]	Input	Async	Link power state request. This signal changes the raw SerDes link/port's power state. When the link/port has completed the transition to the requested power state, the requested state is reflected on PMA_XCVR_POWER_ STATE_ACK. 4'b0000: Idle. 4'b0001: A0 TX/RX active. 4'b0010: A1 Powerdown1 (low power state with minimum exit latency). 4'b000100: A2 Powerdown2 (lower power state with longer exit latency as compared to A1). 4'b1000: A3 Powerdown3 (lower power state and longer exit latency as compared to A2). This is a one hot encoded signal. A subsequent change request shall not be signaled until the current request has been acknowledged and PMA_XCVR_POWER_STATE_REQ has returned to 0. Upon reset release, the first power state must be A2.

Signal	Direction	Clock Domain	Description
SGMII			
GMII_COL	Output	PCS_CLK_RX	MII collision for port *x*. Supports half-duplex operation in 10/100M SGMII mode. Can be ignored in full duplex mode.
GMII_CRS	Output	PCS_CLK_RX	MII carrier sense for port *x*. Supports half-duplex operation in 10/100M SGMII mode. Can be ignored in full duplex mode.
GMII_RX_DV[1:0]	Output	PCS_CLK_RX	GMII receive data valid.
GMII_RX_ER[1:0]	Output	PCS_CLK_RX	GMII receive error.
GMII_RXD[15:0]	Output	PCS_CLK_RX	GMII receive data.
GMII_TX_EN[1:0]	Input	pcs_clk_tx	GMII transmit enable.
GMII_TX_ER[1:0]	Input	PCS_CLK_RX	GMII transmit error.
GMII_TXD[15:0]	Input	pcs_clk_tx	GMII transmit data.
PCS_AN_COMPLETE	Output	apb_clk	Optional status output when SGMII auto-negotiation is defined. Single-cycle interrupt pulse to indicate completion of auto-negotiation for each port (*x*).
SGMII_MODE	Input	Async	2'b00: 10M SGMII mode 2'b01: 100M SGMII mode 2'b10: 1G mode 2'b11: 2.5G mode When set to the 10/100M SGMII modes, the MAC clocks must be slowed down to 10/100th of the speed of the datapath clocks. When set to 2.5G mode, the functionality is the same but the clock speed is more than doubled.

Table 3: Signals per Quad

Signal	Direction	Clock Domain	Description
USER_APB_CLK	Input	N/A	APB clock source, maximum 200 Mhz.
USER_APB_PADDR[23:0]	Input	user_apb_clk	APB address.
USER_APB_PSEL	Input	user_apb_clk	APB select.
USER_APB_PENABLE	Input	user_apb_clk	APB enable.
USER_APB_PWRITE	Input	user_apb_clk	APB write.
USER_APB_PWDATA[31:0]	Input	user_apb_clk	APB write data.
USER_APB_PRDATA[31:0]	Output	user_apb_clk	APB read data.
USER_APB_PREADY	Output	user_apb_clk	APB ready.
PMA_CMN_READY	Output	Async	PMA ready.
LED_TICK_TOGGLE	Input	Async	A toggle signal used for timing LED activity signals for all lanes. This signal should toggle every 0.5 ms.
REM_PRE	Input	Async	Optional 1G control signal. Remove one preamble byte if the number of idles is not even.

Register Map

The following tables show the PCS registers.

Table 4: 1G PCS Register Access

1G PCS Access	Value
USER_APB_PADDR[23:21]	3'b110
USER_APB_PADDR[20:11]	x (Don't care)
USER_APB_PADDR[10:8]	3'b100

Table 5: PCS Port Address Map

Port	USER_APB_PADDR[7:0] Start	USER_APB_PADDR[7:0] End
A	0x00	0x3C
B	0x40	0x7C
C	0x80	0xBC
D	0xC0	0xFC

Table 6: signal_ok Program Bit

Signal	Address	Write Bit
USER_APB_PADDR[23:0]	24'h600040	[14:11] 11: Lane 0 12: Lane 1 13: Lane 2 14: Lane 3

Table 7: Register Map

Register	Type	Reset Value	Address Offset
PCS Control	RW	0x00001040	0x00
PCS Status	RO	0x00000109	0x04
AN Advertised Abilities	RW	0x00000001	0x10
AN LP Abilities	RO	0x00000000	0x14
SGMII CFG1	RW	0x000186A0	0x24
SGMII CFG2	RW	0x000186A0	0x28
Auto Negotiation Extended Status	RO	0x00008000	0x3C

The following tables show the bit description for the PCS registers.

Table 8: PCS Control Register

Bit	Name	Description	Type	Reset
31:16	Reserved	Reserved.	RO	0
15	pcs_software_reset	PCS software reset. Written by software to force the hardware logic into a reset state. This bit is self-clearing. When reading this bit, logic 1 is returned until the reset has. Writing logic 0 has no effect. This bit only resets the AN, TX, and RX GMII state machines.	RW	0
14	loopback_mode	Loopback mode. The ewrap output pin of the PCS reflects this control bit, and can be used to select loopback mode in the PHY transceiver. 0: Loopback mode disabled. 1: Loopback mode enabled	RW	0
13	speed_select_bit_1	Reserved set to 0. Used in conjunction with bit 6 to always indicate 1G operation.	RO	0
12	enable_auto_neg	Enable auto-negotiation. When set active high, auto-negotiation operation is enabled.	RW	1
11:10	reserved	reserved	RO	0
9	restart_auto_neg	Restart auto-negotiation. When set active high, the hardware restarts auto-negotiation. This bit is self-clearing, but once set shall remain in this state until auto-negotiation has restarted. Writing logic 0 has no effect.	RW	0
8	mac_duplex_state	Reserved set to 1. The PCS only supports full duplex operation.	RO	1
7	reserved	Reserved.	RO	0
6	speed_select_bit_0	Reserved set to 1. Used in conjunction with bit 13 to always indicate 1G operation.	RO	1
5:0	reserved	Reserved.	RO	0

Table 9: PCS Status Register

Bit	Name	Description	Type	Reset
31:16	reserved	Reserved.	RO	0
15	base_100_t4	Reserved. Set to 0, not supported.	RO	0
14	base_100_x_full_duplex	Reserved. Set to 0, not supported.	RO	0
13	base_100_x_half_duplex	Reserved. Set to 0, not supported.	RO	0
12	mbps_10_full_duplex	Reserved. Set to 0, not supported.	RO	0
11	mbps_10_half_duplex	Reserved. Set to 0, not supported.	RO	0
10	base_100_t2_full_duplex	Reserved. Set to 0, not supported.	RO	0
9	base_100_t2_half_duplex	Reserved. Set to 0, not supported.	RO	0
8	extended_status	Extended status. When set active high, indicates extended status information is present in the PCS auto-negotiation extended status register. This bit is hardwired to logic 1.	RO	1

Bit	Name	Description	Type	Reset
7:6	reserved	Reserved.	RO	0
5	auto_neg_complete	Auto-negotiation complete. Set active high by the PCS hardware to indicate auto-negotiation has completed.	RO	0
4	remote_fault	Remote fault. Set active high if the link partner remote fault bits in the PCS auto-negotiation link partner ability register, indicates an error. Resets low when read.	RO	0
3	auto_neg_ability	Auto-negotiation ability. This bit indicates whether the PCS has auto-negotiation ability and reflects the value of the auto-negotiation enable bit in the PCS control register. 0: PCS is not able to perform auto-negotiation. 1: PCS is able to perform auto-negotiation	RO	1
2	link_status	Link status. Indicates the status of the physical connection to the link partner. When set to logic 1 the link is up, and when set to logic 0, the link is down. If auto-negotiation is disabled this returns the synchronisation status. Held at logic 0 if the link goes down until this bit is read.	RO	0
1	reserved	Reserved.	RO	0
0	extended_capabilities	Extended register capabilities. When set active high, indicates the PCS supports extended register capabilities. This bit is hardwired to logic 1.	RO	1

Table 10: Auto-Negotiation Advertised Abilities Register

Bits	Name	Description	Type	Reset
31:16	reserved	Reserved.	RO	0
15	reserved	Reserved.	RO	0
14	reserved	Reserved.	RO	0
13:12	reserved	Reserved.	RW	0
11:10	reserved	Reserved.	RO	0
9	reserved	Reserved.	RO	0
8:7	reserved	Reserved.	RW	0
6	reserved	Reserved.	RW	0
5	reserved	Reserved.	RW	1
4:1	reserved	Reserved.	RO	0
0	sgmii_mode	Reserved.	RW	1

Table 11: Auto-Negotiation Link Partner Abilities

Bit	Name	Description	Type	Reset
31:16	reserved	Reserved.	RO	0
15	link_partner	Link status. 0 : Link down. 1 : Link up.	RO	0

Bit	Name	Description	Type	Reset
14	link_partner_acknowledge	Link partner acknowledge. Indicates that the link partner has successfully received the transmitted base page	RO	0
13:12	link_partner_remote_fault_ duplex_mode	Bit 13: Reserved. Read as zero. Bit 12 : Duplex mode.	RO	0
11:9	speed	11: Reserved 10: 1,000 Mbps 01: 100 Mbps 00: 10 Mbps Bit 9: Reserved. Read as zero.	RO	0
8:5	reserved	Reserved. Read as zero.	RO	0
4:0	reserved	Reserved.	RO	0

Table 12: SGMII CFG1

Bit	Name	Description	Type	Reset
31:27	reserved	Reserved.	RO	0
26	uni_direct_en	When set, the auto-negotiation state machine allows the transmit state machine to transmit data when the link is down instead of idle ordered sets.	RW	0
25	alt_sgmii_an_mode	Alternate SGMII mode. When set, along with bit 24, during auto-negotiation configuration data exchange a fixed value of 0x4001 is used for the configuration data.	RW	0
24	sgmii_an_mode	SGMII AN mode. Set to configure auto-negotiation in accordance to SGMII specification.	RW	0
23:21	reserved	Reserved.	RO	0
20:0	an_link_timeout_val	Auto-negotiation link timer timeout value in xcv_rbc clock cycles. This bit should be set to the equivalent 1.6 ms in SGMII mode and 10 ms in other modes.	RW	0x0186A0

Table 13: SGMII CFG2

Bit	Name	Description	Type	Reset
31:21	reserved	Reserved.	RO	0
20:0	an_link_fail_timeout_val	Auto-negotiation link fail timer timeout value in xcv_rbc clock cycles. This bit should be set to the equivalent of 10 ms.	RW	0x0186A0

Table 14: Auto-Negotiation Extended Status

Bit	Name	Description	Type	Reset
31:16	reserved	Reserved.	RO	0
15	full_duplex_1000base_x	Full duplex 1000BASE-X. Hardwired to logic 1, indicates the PCS can support full duplex operation of 1000BASE-X.	RO	1

Bit	Name	Description	Type	Reset
14	half_duplex_1000base_x	Half duplex 1000BASE-X. Hardwired to logic 0, indicates the PCS cannot support half duplex operation of 1000BASE-X.	RO	0
13	full_duplex_1000base_t	Full duplex 1000BASE-T. Hardwired to logic 0, indicates the PCS cannot support 1000BASE-T full duplex operation.	RO	0
12	half_duplex_1000base_t	Half duplex 1000BASE-T. Hardwired to logic 0, indicates the PCS cannot support 1000BASE-T half duplex operation.	RO	0
11:0	reserved	Reserved.	RO	0

Table 15: 1G PCS Lane Configuration

Bit	Name	Description	Type	Reset
31:19	reserved	Reserved.	RO	0
18:15	cfg_sgmii_clkdiv_en_p0 cfg_sgmii_clkdiv_en_p1 cfg_sgmii_clkdiv_en_p2 cfg_sgmii_clkdiv_en_p3	Auto-negotiation clock rate change enable: 18: Lane 3 17: Lane 2 16: Lane 1 15: Lane 0	RW	1[(1)]
14:11	signal_ok	PCS signal_ok program bit. To start the PCS RX operation: 14: Lane 3 13: Lane 2 12: Lane 1 11: Lane 0	RW	0
10:9	test_sel	Selects the test pattern to be transmitted: 00: High-frequency Test Pattern (0101010101010101..) 01: Low-frequency Test Pattern (11111000001111100..) 10: Mixed-frequency Test Pattern (1111101011000000..) 11: Reserved	RW	0
8	test_enable	Enables the transmission of the selected test pattern.	RW	0
7:4	polarity_inv_tx	Invert 20-bit polarity on transmit: 7: Lane3 6: Lane2 5: Lane1 4: Lane0	RW	0
3:0	polarity_inv_rx	Invert 20-bit polarity on receive: 3: Lane3 2: Lane2 1: Lane1 0: Lane0	RW	0

(1) Change to 1 in HWTCL.

To program the special PCS lanes configuration in Table 15: 1G PCS Lane Configuration on page 16, use the following APB address:

- USER_APB_PADDR[23:0]—24'h600040

Revision History

Table 16: Document Revision History

Date	Version	Description
January 2025	1.0	Initial release.