Titanium Quarterly Ongoing Reliability Monitoring Report

TiORM-v4.0
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Introduction

Efinix® Titanium™ FPGAs feature a programmable logic and routing fabric built with the Quantum™ architecture. The Titanium platform consists of ten devices, built on TSMC's 16nm process, with a logic density range from 35K to 1M logic elements (LEs) and standard interfaces such as GPIO, PLLs, oscillators, MIPI, DDR, LVDS, PCI Express, etc.

This ongoing reliability monitoring (ORM) report is used to measure the reliability of all devices built on TSMC's 16nm process technology on a regular basis.

Ongoing Reliability Monitoring Requirements

Table 1: Ongoing Reliability Monitoring Requirements

Refer to the data in the following sections for the sample size for each condition

Reliability Test	Purpose	Reference Standard	Test Condition	Sample Size / Frequency
Moisture Sensitivity Level (MSL) Pre-conditioning (PC) (per Package MSL Level)	To simulate the thermal & mechanical stresses imposed on a device when mounted on PCB.	J-STD-020 JESD22-A113	Bake at 125°C, 24hrs, Per Package MSL Level, 3x reflow @ 260°C	All units included in TC & uHAST
Temperature Cycling (TC)	To evaluate the package & die interface mechanical resistance to alternate exposures of high & low temperature changes. Evaluate stress integrity of die attach to lead frame & wire bond to die and lead.	JESD22-A104	-55°C to 125°C or -55°C to 150°C 500 & 1000 cycles	Min. 45 units per quarter
High Temperature Storage Life (HTSL)	To evaluate the package under storage condition with the effect of time and temperature.	JESD22-A103	150°C 168, 500 & 1000 hours	Min. 45 units per quarter
Highly Accelerated Stress Test (uHAST)	To evaluate the reliability of mold compound (plastic) and laminate (BGA) integrated circuits packages in non-condensing moisture or humid conditions.	JESD22-A118	130°C /85% RH 96 & 192 hours	Min. 45 units per quarter
High Temperature Operating Life (HTOL)	To simulate the end-user part application over early, inherent, or extended life period of the product.	JESD22-A108	Tj 125°C 168, 500 & 1000 hours	Min. 45 units per quarter

ORM Data

This section describes the results of ORM.

High-Temperature Operating Life (HTOL)

Table 2: HTOL Data

Device	Package	Tech Node	Quantity	Failures		
				168hrs	500hrs	1000hrs
Ti180	FCCSP 484	TSMC 16nm	154	0	0	0
Ti60	FBGA 225	TSMC 16nm	231	0	0	0

MSL Preconditioning Testing (PC)

Table 3: PC Data

Device	Package	Tech Node	Quantity	Failures
				MSL3
Ti180	FCCSP 484	TSMC 16nm	308	0
Ti180	FCCSP 361	TSMC 16nm	77	0
Ti180	HFCBGA 529	TSMC 16nm	77	0
Ti180	FCCSP 400	TSMC 16nm	77	0
Ti60	FBGA 225	TSMC 16nm	462	0

Temperature Cycling (TC)

Table 4: TC Data

Device	Package	Tech Node	Quantity	Failures	
				500 cycs	1000 cycs
Ti180	FCCSP 484	TSMC 16nm	154	0	0
Ti60	FBGA 225	TSMC 16nm	231	0	0

Unbiased HAST (uHAST)

Table 5: uHAST Data

Device	Package	Tech Node	Quantity	Failures	
				96hrs	192hrs
Ti180	FCCSP 484	TSMC 16nm	154	0	0
Ti180	FCCSP 361	TSMC 16nm	77	0	0
Ti180	HFCBGA 529	TSMC 16nm	77	0	0
Ti180	FCCSP 400	TSMC 16nm	77	0	0
Ti60	FBGA 225	TSMC 16nm	231	0	0

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High-Temperature Storage Life (HTSL)

Table 6: HTSL Data

Device	Package	Tech Node	Quantity	Failures		
				168hrs	500hrs	1000hrs
Ti180	FCCSP 484	TSMC 16nm	154	0	0	0
Ti60	FBGA 225	TSMC 16nm	231	0	0	0

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Failure Rate Estimation by Fab Technology

Failure in Time (FIT)

A long-term, steady-state failure rate is often required by circuit and system engineers for allocations of the failure rates at the component level during system design. FIT, which stands for failure-in-time, is a widely used term to describe failure rates of electronic components, and as used here, represents the number of failures in a billion hours of operation.

Failure Rate Calculation Method

Long-term failure rates are estimated by applying the Arrhenius equation to data collected from long term operating life tests. A confidence factor is applied based upon the sample size and number of failures to estimate the maximum failure rate at a specific confidence level.

$$FITRate = \frac{(\chi^2/2)\times 10^9}{\text{Accelerated Stress Device Hours}}$$

Table 7: FIT Data

The failure rate prediction for TSMC 16nm family products, with activation energy of 0.7eV, and with ambient operating temperature (Ta) as below.

FAILURE RATE	C.L. = 60%	C.L. = 70%
Ta (°C)	**FIT**	**FIT**
55°C	5.8	7.6

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Revision History

Date	Version	Description
December 2024	1.0	Initial release.
April 2025	2.0	Add in Q3'2024 ORM result for Ti180 FCCSP484 and Ti60 FBGA225.
July 2025	3.0	Add in Q4'2024 ORM result for Ti60 FBGA225.
November 2025	4.0	Add in Q1'2025 ORM result for Ti60 FBGA225.

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