



Ruby RISC-V SoC Data Sheet

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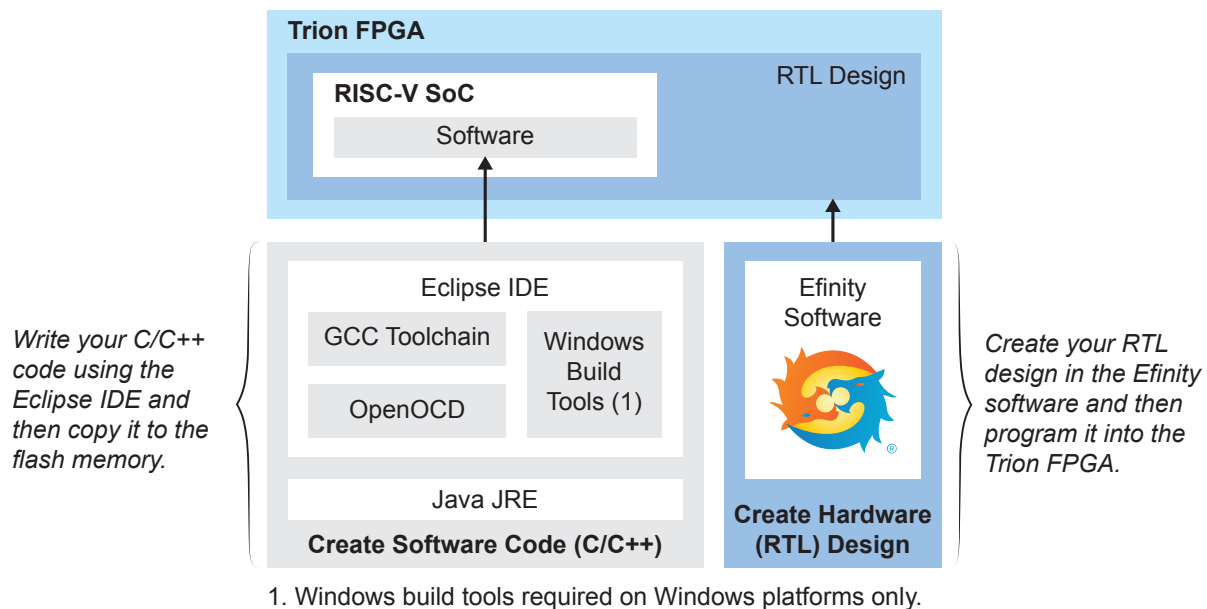
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Introduction

Efnix provides the heavy-weight, cached soft RISC-V SoC, Ruby, which includes a DDR DRAM controller interface. This SoC is ideal for applications that use triple-speed Ethernet and communications protocols, provide real-time system controls, and perform image signal processing. Some example applications for the Ruby SoC are embedded vision, industrial control, and multiple microphone voiceprint recognition, which require high performance with hardware acceleration. This core is similar to the open-source SaxonSOC, but it has been optimized for Trion® FPGAs.

Figure 1: Ruby RISC-V SoC Design Flow



Learn more: For details on developing RTL designs or creating software, refer to the [Ruby RISC-V Hardware and Software User Guide](#).

VexRiscv RISC-V Core

The Ruby SoC is based on the VexRiscv core created by Charles Papon. The VexRiscv core is a 32-bit CPU using the ISA RISC-V32I with M and C extensions, has five pipeline stages (fetch, decode, execute, memory, and writeback), and a configurable feature set. In the Ruby SoC, the VexRiscv core supports the AXI4 and APB3 bus interfaces, has instruction and data caches, and can run at speeds up to 1.16 DMIPS/MHz.

The VexRiscv core won first place in the RISC-V SoftCPU contest in 2018.⁽¹⁾

⁽¹⁾ <https://www.businesswire.com/news/home/20181206005747/en/RISC-V-SoftCPU-Contest-Winners-Demonstrate-Cutting-Edge-RISC-V>

Features

- VexRiscv processor with 5 pipeline stages (fetch, decode, execute, memory, and write back), interrupts and exception handling with machine mode
 - 4 KB data cache
 - 4 KB instruction cache
- 50 MHz system clock frequency
- 4 KB on-chip RAM with boot loader for SPI flash
- DDR controller
 - 100 MHz DDR memory bus frequency
 - 128-bit AXI data width
 - 3.5 GB memory module
 - 400 MHz DDR clock frequency, 800 Mbps
- 1 AXI master channel to access the DDR memory
- 1 AXI slave channel to user logic
- APB3 peripherals:
 - 16 GPIOs
 - 3 I²C masters and slaves
 - Machine timer
 - PLIC
 - 3 SPI flash masters with a maximum clock frequency of 25 MHz
 - 2 UARTs with 115,200 baud rate
 - 2 slave user peripherals

FPGA Support

The Ruby SoC supports T35, T55, T85, and T120 Trion[®] FPGAs.

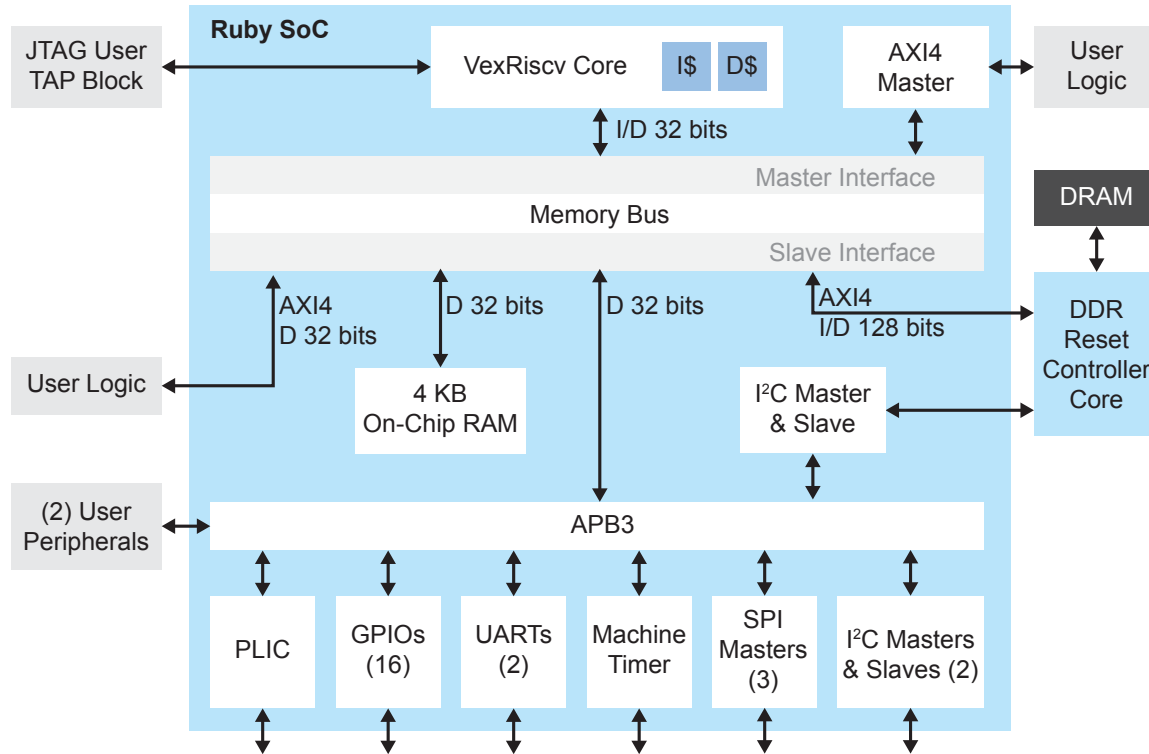
Resource Utilization and Performance

FPGA	Logic Utilization (LUTs)	Memory Blocks	f _{MAX} (MHz)	Language	Efinity Version
T120 BGA324 C4	12,093	78	SoC: 53.229 DDR: 100	Verilog HDL	2019.3

Functional Description

The Ruby SoC incorporates a 32-bit RISC-V processor, 4 KB instruction cache, 4 KB data cache, 4 KB of on-chip RAM, and a variety of peripherals (including 2 APB3 slave peripherals and 1 AXI slave). The SoC includes 3 I²C peripherals and a 128-bit half-duplex AXI bus to communicate with the Efinix DDR controller core. This core uses the Trion[®] FPGAs hard DDR DRAM interface to reset an external DRAM module (resets and re-initializes the Trion[®] FPGA's DDR interface as well as the DDR module(s)).

Figure 2: Ruby SoC Block Diagram



Address Map

Table 1: Default Address Map, Interrupt ID, and Cached Channels

The AXI user slave channel is in a cacheless region (I/O) for compatibility with AXI-Lite.

Device	Address	Size	Interrupt ID	Region
Null	0x0000_0FFF - 0x0000_0000	4K	-	-
Off-chip DRAM	0xF7FF_FFFF - 0x0000_1000	3.5 GBytes	-	Cache
GPIO	0xF800_0FFF - 0xF800_0000	4K	[0]: 12 [1]: 13	I/O
I ² C 0	0xF801_8FFF - 0xF801_8000	4K	8	I/O
I ² C 1	0xF801_9FFF - 0xF801_9000	4K	9	I/O
I ² C 2	0xF801_AFFF - 0xF801_A000	4K	10	I/O
Machine timer	0xF800_8FFF - 0xF800_8000	4K	31	I/O
PLIC	0xF8C0_0FFF - 0xF8C0_0000	4K	-	I/O
SPI master 0	0xF801_4FFF - 0xF801_4000	4K	4	I/O
SPI master 1	0xF801_5FFF - 0xF801_5000	4K	5	I/O
SPI master 2	0xF801_6FFF - 0xF801_6000	4K	6	I/O
UART 0	0xF801_0FFF - 0xF801_0000	4K	1	I/O
UART 1	0xF801_1FFF - 0xF801_1000	4K	2	I/O
User peripheral 0	0xF880_0FFF - 0xF880_0000	4K	-	I/O
User peripheral 1	0xF880_1FFF - 0xF880_1000	4K	-	I/O
On-chip BRAM	0xF900_0FFF - 0xF900_0000	4K	-	Cache
AXI user slave	0xFA00_0FFF - 0xFA00_0000	4K	-	I/O
External interrupt	-	-	25	I/O



Note: The RISC-V GCC compiler does not support user address spaces starting at 0x0000_0000.

Flash Address

When the FPGA boots up, the Ruby SoC copies your binary application file from a SPI flash device to the DDR DRAM module, and then begins execution.

The SPI flash binary address starts at 0x0038_0000.

Clocks

Table 2: Clock Ports

Port	Direction	Description
io_systemClock	Input	Provides a 50 MHz clock for the SoC.
io_memoryClock	Input	Provides a 100 MHz clock for the DDR DRAM memory bus.

Interrupts

Table 3: Interrupt Ports

Port	Direction	Description
userInterruptA	Input	Provides an external interrupt.
io_axiAInterrupt	Input	User AXI slave channel interrupt.

Resets

The Ruby SoC has a master reset signal, `io_asyncReset` that triggers a system reset. Your RTL design should hold `io_asyncReset` for 10 ns to reset the whole SoC system completely. When you assert `io_asyncReset`, the SoC asserts:

- `io_systemReset`, which resets the RISC-V processor, on-chip memory, and peripherals
- `io_memoryReset`, which resets the DDR controller, DRAM module, I²C master and slave connected to the DDR reset controller core, and any user logic
- `io_ddrMasters_0_reset`, which responds to the reset for each DDR master and is synchronized to the `io_ddrMasters_0_clk`

The SoC asserts the `io_memoryReset` and `io_ddrMaster_0_reset` signals at the same time to allow the AXI masters access to the AXI cross bar once the reset completes.

Once `io_systemReset` goes low, the user binary code is executed.

Table 4: Reset Ports

Port	Direction	Description
io_asyncReset	Input	Active-high asynchronous reset for the entire system.
io_systemReset	Output	Synchronous active-high reset for systemClk.
io_memoryReset	Output	DDR reset source from the RISC-V SoC.
io_ddrMasters_0_reset	Output	Responds to the reset for the DDR master.

AXI Interface

The Ruby SoC has a 128-bit slave interface to communicate with the DDR controller core. Additionally it has an AXI slave to connect to user logic. The AXI user slave channel is compatible with AXI-Lite. Refer to the AMBA AXI and ACE Protocol Specification for AXI channel descriptions and handshake information.

AXI Interface to DDR DRAM

Table 5: DDR Slave Half-Duplex Address Channel for Read and Write

Port	Direction	Description
io_ddrA_arw_valid	Output	DDR address valid.
io_ddrA_arw_ready	Input	DDR address ready.
io_ddrA_arw_payload_addr[31:0]	Output	DDR address.
io_ddrA_arw_payload_id[7:0]	Output	DDR address ID.
io_ddrA_arw_payload_region[3:0]	Output	DDR region identifier.
io_ddrA_arw_payload_len[7:0]	Output	DDR burst length.
io_ddrA_arw_payload_size[2:0]	Output	DDR burst size.
io_ddrA_arw_payload_burst[1:0]	Output	DDR burst type, INCR only.
io_ddrA_arw_payload_lock	Output	DDR lock type.
io_ddrA_arw_payload_cache[3:0]	Output	DDR memory type.
io_ddrA_arw_payload_qos[3:0]	Output	DDR quality of service.
io_ddrA_arw_payload_prot[2:0]	Output	DDR protection type.
io_ddrA_arw_payload_write	Output	DDR address read/write selection: 0: Read 1: Write

Table 6: DDR Slave Write Data Channel

Port	Direction	Description
io_ddrA_w_valid	Output	DDR write valid.
io_ddrA_w_ready	Input	DDR write ready.
io_ddrA_w_payload_data[127:0]	Output	DDR write data.
io_ddrA_w_payload_strb[15:0]	Output	DDR write strobe.
io_ddrA_w_payload_last	Output	DDR write last.

Table 7: DDR Slave Write Respond Channel

Port	Direction	Description
io_ddrA_b_valid	Input	DDR write respond valid.
io_ddrA_b_ready	Output	DDR respond ready.
io_ddrA_b_payload_id[7:0]	Input	DDR respond ID.
io_ddrA_b_payload_resp[1:0]	Input	DDR write respond.

Table 8: DDR Slave Read Data Channel

Port	Direction	Description
io_ddrA_r_valid	Input	DDR read valid.
io_ddrA_r_ready	Output	DDR read ready.
io_ddrA_r_payload_data[127:0]	Input	DDR read data.
io_ddrA_r_payload_id[7:0]	Input	DDR read ID.
io_ddrA_r_payload_resp[1:0]	Input	DDR read respond.
io_ddrA_r_payload_last	Input	DDR read last.

AXI Interface to User Logic

Table 9: User Slave Write Address Channel

Port	Direction	Description
axiA_awvalid	Output	User write address valid.
axiA_awready	Input	User write address ready.
axiA_awaddr[31:0]	Output	User write address.
axiA_awid[7:0]	Output	User write address ID.
axiA_awregion[3:0]	Output	User region identifier.
axiA_awlen[7:0]	Output	User burst length.
axiA_awsz[2:0]	Output	User burst size.
axiA_awburst[1:0]	Output	User burst type, INCR only.
axiA_awlock	Output	User lock type.
axiA_awcache[3:0]	Output	User memory type.
axiA_awqos[3:0]	Output	User quality of service.
axiA_awprot[2:0]	Output	User protection type.

Table 10: User Slave Write Data Channel

Port	Direction	Description
axiA_wvalid	Output	User write valid.
axiA_wready	Input	User write ready.
axiA_wdata[127:0]	Output	User write data.
axiA_wstrb[15:0]	Output	User write strobe.
axiA_wlast	Output	User write last.

Table 11: User Slave Write Respond Channel

Port	Direction	Description
axiA_bvalid	Input	User write respond valid.
axiA_bready	Output	User respond ready.
axiA_bid[7:0]	Input	User respond ID.
axiA_bresp[1:0]	Input	User write respond.

Table 12: User Slave Read Address Channel

Port	Direction	Description
axiA_arvalid	Output	User read address valid.
axiA_arready	Input	User read address ready.
axiA_araddr[31:0]	Output	User read address.
axiA_arid[7:0]	Output	User read address ID.
axiA_arregion[3:0]	Output	User region identifier.
axiA_arlen[7:0]	Output	User burst length.
axiA_arsize[2:0]	Output	User burst size.
axiA_arburst[1:0]	Output	User burst type, INCR only.
axiA_arlock	Output	User lock type.
axiA_arcache[3:0]	Output	User memory type.
axiA_arqos[3:0]	Output	User quality of service.
axiA_arprot[2:0]	Output	User protection type.

Table 13: User Slave Read Data Channel

Port	Direction	Description
axiA_rvalid	Input	User read valid.
axiA_rready	Output	User read ready.
axiA_rdata[127:0]	Input	User read data.
axiA_rid[7:0]	Input	User read ID.
axiA_rresp[1:0]	Input	User read respond.
axiA_rlast	Input	User read last.

Table 14: User Master Clock and Reset

Port	Direction	Description
io_ddrMasters_0_clk	Input	AXI master clock.
io_ddrMasters_0_reset	Output	AXI master active high reset.

AXI Master Interface

Table 15: User Master Write Address Channel

Port	Direction	Description
io_ddrMasters_0_aw_valid	Input	User write address valid.
io_ddrMasters_0_aw_ready	Output	User write address ready.
io_ddrMasters_0_aw_payload_addr[31:0]	Input	User write address.
io_ddrMasters_0_aw_payload_id[7:0]	Input	User write address ID.
io_ddrMasters_0_aw_payload_region[3:0]	Input	User region identifier.
io_ddrMasters_0_aw_payload_len[7:0]	Input	User burst length.
io_ddrMasters_0_aw_payload_size[2:0]	Input	User burst size.

Port	Direction	Description
io_ddrMasters_0_aw_payload_burst[1:0]	Input	User burst type, INCR only.
io_ddrMasters_0_aw_payload_lock	Input	User lock type.
io_ddrMasters_0_aw_payload_cache[3:0]	Input	User memory type.
io_ddrMasters_0_aw_payload_qos[3:0]	Input	User quality of service.
io_ddrMasters_0_aw_payload_prot[2:0]	Input	User protection type.

Table 16: User Master Write Data Channel

Port	Direction	Description
io_ddrMasters_0_w_valid	Input	User write valid.
io_ddrMasters_0_w_ready	Output	User write ready.
io_ddrMasters_0_w_payload_data[127:0]	Input	User write data.
io_ddrMasters_0_w_payload_strb[15:0]	Input	User write strobe.
io_ddrMasters_0_w_payload_last	Input	User write last.

Table 17: User Master Write Respond Channel

Port	Direction	Description
io_ddrMasters_0_b_valid	Output	User write respond valid.
io_ddrMasters_0_b_ready	Input	User respond ready.
io_ddrMasters_0_b_payload_id[7:0]	Output	User respond ID.
io_ddrMasters_0_b_payload_resp[1:0]	Output	User write respond.

Table 18: User Master Read Address Channel

Port	Direction	Description
io_ddrMasters_0_ar_valid	Input	User read address valid.
io_ddrMasters_0_ar_ready	Output	User read address ready.
io_ddrMasters_0_ar_payload_addr[31:0]	Input	User read address.
io_ddrMasters_0_ar_payload_id[7:0]	Input	User read address ID.
io_ddrMasters_0_ar_payload_region[3:0]	Input	User region identifier.
io_ddrMasters_0_ar_payload_len[7:0]	Input	User burst length.
io_ddrMasters_0_ar_payload_size[2:0]	Input	User burst size.
io_ddrMasters_0_ar_payload_burst[1:0]	Input	User burst type, INCR only.
io_ddrMasters_0_ar_payload_lock	Input	User lock type.
io_ddrMasters_0_ar_payload_cache[3:0]	Input	User memory type.
io_ddrMasters_0_ar_payload_qos[3:0]	Input	User quality of service.
io_ddrMasters_0_ar_payload_prot[2:0]	Input	User protection type.

Table 19: User Master Read Data Channel

Port	Direction	Description
io_ddrMasters_0_r_valid	Output	User read valid.
io_ddrMasters_0_r_ready	Input	DDR read ready.
io_ddrMasters_0_r_payload_data[127:0]	Output	DDR read data.
io_ddrMasters_0_r_payload_id[7:0]	Output	DDR read ID.
io_ddrMasters_0_r_payload_resp[1:0]	Output	DDR read respond.
io_ddrMasters_0_r_payload_last	Output	DDR read last.

APB3 Interface

The following table shows the ports for the APB3 user slave peripherals. Refer to the AMBA APB Protocol Specification for APB port descriptions and handshake information.

Table 20: APB3 Ports

Where n is 0 or 1

Port	Direction	Description
io_apbSlave_n_PADDR[11:0]	Output	User address.
io_apbSlave_n_PSEL	Output	User select.
io_apbSlave_n_PENABLE	Output	User enable.
io_apbSlave_n_PREADY	Input	User ready.
io_apbSlave_n_PWRITE	Output	User direction.
io_apbSlave_n_PWDATA[31:0]	Output	User write data.
io_apbSlave_n_PRDATA[31:0]	Input	User read data.
io_apbSlave_n_PSLVERROR	Input	User transfer failure.

JTAG Interface

The Ruby SoC uses the JTAG User TAP interface block to communicate with the OpenOCD debugger.

Table 21: JTAG Ports

Port	Direction	Description
jtagCtrl_enable	Input	Indicates that the user instruction is active for the interface.
tagCtrl_capture	Input	TAP controller is in the capture state.
jtagCtrl_shift	Input	TAP controller is in the shift state.
jtagCtrl_update	Input	TAP controller in the update state.
jtagCtrl_reset	Input	TAP controller is in the reset state.
jtagCtrl_tdi	Input	JTAG TDI for debugging.
jtagCtrl_tdo	Output	JTAG TDO for debugging.
jtagCtrl_tck	Input	JTAG TCK for debugging.

GPIO Peripheral Interface

The GPIO interface starts at address 0xF800_0000.

Table 22: GPIO Ports

Port	Direction	Description
system_gpio_0_io_read[15:0]	Input	GPIO input.
system_gpio_0_io_write[15:0]	Output	GPIO output.
system_gpio_0_io_writeEnable[15:0]	Output	GPIO output enable.

Table 23: GPIO Register Map

Address Offset	Register Name	Privilege	Width
0x0000_0000	Input	Read/Write	32
0x0000_0004	Output	Read/Write	32
0x0000_0008	Output Enable	Read/Write	32
0x0000_0020	Interrupt Rise Enable	Read/Write	32
0x0000_0024	Interrupt Fall Enable	Read/Write	32
0x0000_0028	Interrupt High Enable	Read/Write	32
0x0000_002C	Interrupt Low Enable	Read/Write	32

Input Register: 0x0000_0000

31	0
Input	

Bits	Field	Description	Privilege
0-31	Input	Set GPIO pin as an input (32 pins).	Read/Write

Output Register: 0x0000_0004

31	0
Output	

Bits	Field	Description	Privilege
0-31	Output	Set GPIO pin as an output (32 pins).	Read/Write

Output Enable Register: 0x0000_0008

31	0
OE	

Bits	Field	Description	Privilege
0-31	OE	Enable GPIO output pin (32 pins).	Read/Write

Interrupt Rise Enable Register: 0x0000_0020

31	0
IntRiseEn	

Bits	Field	Description	Privilege
0-31	IntRiseEn	Enable a rise interrupt on the GPIO pin (32 pins).	Read/Write

Interrupt Fall Enable Register: 0x0000_0024

31	0
IntFallEn	

Bits	Field	Description	Privilege
0-31	IntFallEn	Enable a fall interrupt on the GPIO pin (32 pins).	Read/Write

Interrupt High Enable Register: 0x0000_0028

31	0
IntHighEn	

Bits	Field	Description	Privilege
0-31	IntHighEn	Enable a high interrupt on the GPIO pin (32 pins).	Read/Write

Interrupt Low Enable Register: 0x0000_002C

31	0
IntLowEn	

Bits	Field	Description	Privilege
0-31	IntLowEn	Enable a low interrupt on the GPIO pin (32 pins).	Read/Write

I²C Peripheral Interface

The Ruby SoC has 3 I²C master/slave peripherals. You use the `system_i2c_2*` ports to calibrate the DDR DRAM memory; if you do not want to perform calibration, you can use this peripheral for your own purposes. The I²C interface starts at these addresses:

- I²C 0—0xF801_8000
- I²C 1—0xF801_9000
- I²C 2—0xF801_A000

Table 24: I²C Peripheral Ports (User)

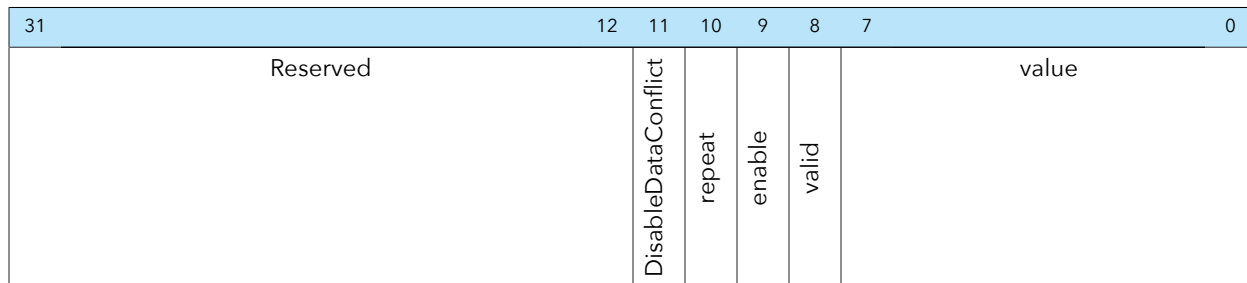
Where *n* is 0, 1, or 2.

Port	Direction	Description
<code>system_i2c_n_io_sda_write</code>	Output	SDA output for user device.
<code>system_i2c_n_io_sda_read</code>	Input	SDA input for user device.
<code>system_i2c_n_io_scl_write</code>	Output	SCL output for user device.
<code>system_i2c_n_io_scl_read</code>	Input	SCL input for user device.

Table 25: I²C Register Map

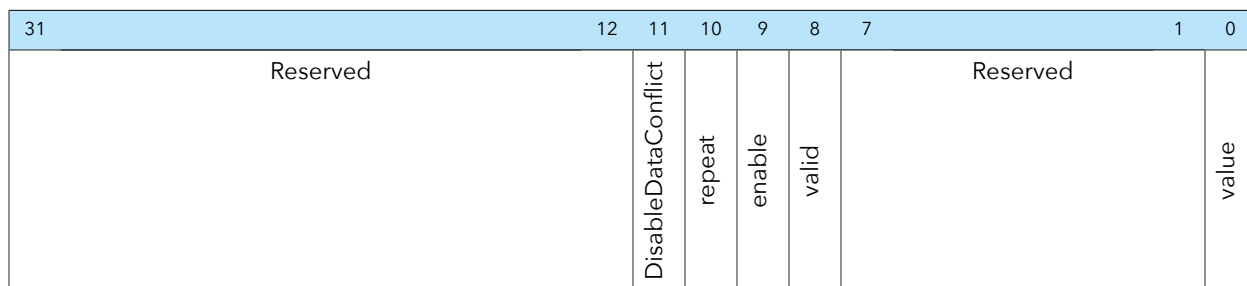
Address Offset	Register Name	Privilege	Width
0x0000_0000	txData	Read/Write	32
0x0000_0004	txAck	Read/Write	32
0x0000_0008	rxData	Read/Write	32
0x0000_000C	rxAck	Read/Write	32
0x0000_0020	Interrupt	Read/Write	32
0x0000_0024	Interrupt Clears	Read/Write	32
0x0000_0028	Sampling Clock Divider	Read/Write	32
0x0000_002C	Timeout	Write	32
0x0000_0030	tsuData	Write	32
0x0000_0040	Master Status	Read/Write	32
0x0000_0050	tlow	Read/Write	32
0x0000_0054	tHigh	Read/Write	32
0x0000_0058	tBuf	Read/Write	32
0x0000_0080	Filtering Status	Read/Write	32
0x0000_0084	Hit Context	Read/Write	32
0x0000_0088	Filtering Configuration	Read/Write	32

txData Register: 0x0000_0000



Bits	Field	Description	Privilege
0-7	value	Transmit data value.	Write
8	valid	Transmit data valid bit.	Read/Write
9	enable	Transmit data enable.	Read/Write
10	repeat	Transmit data repeat bit.	Write
11	DisableDataConflict	Disable transmit data conflict.	Write
12-31	Reserved	Reserved.	N/A

txAck Register: 0x0000_0004



Bits	Field	Description	Privilege
0	value	Transmit acknowledge bit.	Write
1-7	Reserved	Reserved.	N/A
8	valid	Transmit acknowledge valid bit.	Read/Write
9	enable	Transmit acknowledge enable.	Read/Write
10	repeat	Transmit acknowledge repeat bit.	Write
11	DisableDataConflict	Disable transmit acknowledge conflict.	Write
12-31	Reserved	Reserved.	N/A

rxData Register: 0x0000_0008

31	10	9	8	7	0
Reserved			listen	valid	value

Bits	Field	Description	Privilege
0-7	value	Received data.	Read
8	valid	Receive data valid.	Read
9	listen	Start listen data.	Write
10-31	Reserved	Reserved.	N/A

rxAck Register: 0x0000_000C

31	10	9	8	7	1	0
Reserved			listen	valid	Reserved	value

Bits	Field	Description	Privilege
0	value	Received acknowledge.	Read
1-7	Reserved	Reserved.	N/A
8	valid	Receive acknowledge valid.	Read
9	listen	Start listen acknowledge.	Write
10-31	Reserved	Reserved.	N/A

Interrupt Register: 0x0000_0020

31	22	21	20	19	18	17	16	15	12	11	10	9	8	7	6	5	4	3	2	1	0		
Reserved			filterFlag	clockGenBusyFlag	Reserved		filterEnable	clockGenBusyEnable	Reserved			dropFlag	endFlag	restartFlag	startFlag	dropEnable	endEnable	restartEnable	startEnable	txAckEnable	txDataEnable	rxAckEnable	rxDataEnable

Bits	Field	Description	Privilege
0	rxDataEnable	Receive data interrupt enable	Read/Write
1	rxAckEnable	Receive acknowledge interrupt enable	Read/Write
2	txDataEnable	Transmit data interrupt enable	Read/Write
3	txAckEnable	Transmit acknowledge interrupt enable	Read/Write
4	startEnable	Start interrupt enable	Read/Write
5	restartEnable	Restart interrupt enable	Read/Write
6	endEnable	End interrupt enable	Read/Write
7	dropEnable	Drop interrupt enable	Read/Write
8	startFlag	Start interrupt flag	Read
9	restartFlag	Restart interrupt flag	Read
10	endFlag	End interrupt flag	Read
11	dropFlag	Drop interrupt flag	Read
12-15	Reserved	Reserved.	N/A
16	clockGenBusyEnable	Master clock generation interrupt enable.	Read/Write
17	filterEnable	Slave address filtering hit interrupt enable	Read/Write
18-19	Reserved	Reserved.	N/A
20	clockGenBusyFlag	Master clock generation interrupt flag.	Read
21	filterFlag	Slave address filtering hit interrupt flag.	Read
22-31	Reserved	Reserved.	N/A

Interrupt Clears Register: 0x0000_0024

31	12	11	10	9	8	7	0		
Reserved				dropFlagClear	endFlagClear	restartFlagClear	startFlagClear	Reserved	

Bits	Field	Description	Privilege
0-7	Reserved	Reserved.	N/A
8	startFlagClear	Clear start flag.	Write
9	restartFlagClear	Clear restart flag.	Write
10	endFlagClear	Clear end flag.	Write
10	dropFlagClear	Clear drop flag.	Write
12-31	Reserved	Reserved.	N/A

Timeout Register: 0x0000_002C

31	20	19	0
Reserved		value	

Bits	Field	Description	Privilege
0-19	value	Inactive timeout setting.	Write
20-31	Reserved	Reserved.	N/A

Sampling Clock Divider Register: 0x0000_0028

31	10	9	0
Reserved		samplingClockDividerWidth	

Bits	Field	Description	Privilege
0-9	samplingClockDividerWidth	Clock divider width. Controls the rate at which the I ² C controller reads SCL and SDA.	Read/Write
10-31	Reserved	Reserved.	N/A

tsuData Register: 0x0000_0030

31	6	5	0
Reserved		value	

Bits	Field	Description	Privilege
0-5	value	Data setup time.	Write
6-31	Reserved	Reserved.	N/A

Master Status Register: 0x0000_0040

31	7	6	5	4	3	1	0
Reserved				drop	stop	start	Reserved
							isBusy

Bits	Field	Description	Privilege
0	isBusy	Master busy.	Read
1-3	Reserved	Reserved.	N/A
4	start	Master start.	Read/Write
5	stop	Master stop.	Read/Write
6	drop	Master drop.	Read/Write
6-31	Reserved	Reserved.	N/A

tLow Register: 0x0000_0050

31	12	11	0
Reserved		value	

Bits	Field	Description	Privilege
0-11	value	SCL low period.	Write
12-31	Reserved	Reserved.	N/A

tHigh Register: 0x0000_0054

31	12	11	0
Reserved		value	

Bits	Field	Description	Privilege
0-11	value	SCL high period.	Write
12-31	Reserved	Reserved.	N/A

tBuf Register: 0x0000_0058

31	12	11	0
Reserved		value	

Bits	Field	Description	Privilege
0-11	value	Start and stop bus free time.	Write
12-31	Reserved	Reserved.	N/A

Filtering Status Register: 0x0000_0080

31	8	7	6	5	4	3	2	1	0		
Reserved				hit_7	hit_6	hit_5	hit_4	hit_3	hit_2	hit_1	hit_0

Bits	Field	Description	Privilege
0	hit_0	Filtering hit bit 0.	Read
1	hit_1	Filtering hit bit 1.	Read
2	hit_2	Filtering hit bit 2.	Read
3	hit_3	Filtering hit bit 3.	Read
4	hit_4	Filtering hit bit 4.	Read
5	hit_5	Filtering hit bit 5.	Read
6	hit_6	Filtering hit bit 6.	Read
7	hit_7	Filtering hit bit 7.	Read
8-32	Reserved	Reserved.	N/A

Hit Context Register: 0x0000_0084

31	1	0
Reserved		rw

Bits	Field	Description	Privilege
0	rw	Hit context read.	Read
1-31	Reserved	Reserved.	N/A

PLIC Peripheral Interface

The PLIC interface starts at address 0xF8C0_0000.

Table 26: RISC-V PLIC Operation Parameters

Defines	Description
Interrupt priorities registers	The interrupt priority for each interrupt source.
Interrupt pending bits registers	The interrupt pending status of each interrupt source.
Interrupt enables registers	Enables the interrupt source of each context.
Priority thresholds registers	The interrupt priority threshold of each context.
Interrupt claim registers	The register to acquire interrupt source ID of each context.
Interrupt completion registers	The register to send interrupt completion message to the associated gateway.

SPI Master Peripheral Interface

The SPI master peripheral interface supports traditional 4-wire SPI as well as quad-SPI mode, which sends 4 data bits per clock cycle. When implementing the SPI peripheral in traditional dual-line mode, use the `data_0` ports as MOSI and the `data_1` ports as MISO.

The SPI master interface starts at address:

- SPI master 0—0xF801_4000
- SPI master 1—0xF801_5000
- SPI master 2—0xF801_6000

Table 27: SPI Master Ports

Where n is 0, 1, or 2

Port	Direction	Description
<code>system_spi_n_io_sclk_write</code>	Output	SPI SCK.
<code>system_spi_n_io_data_0_writeEnable</code>	Output	SPI output enable for data 0.
<code>system_spi_n_io_data_0_read</code>	Input	SPI input for data 0.
<code>system_spi_n_io_data_0_write</code>	Output	SPI output for data 0.
<code>system_spi_n_io_data_1_writeEnable</code>	Output	SPI output enable for data 1.
<code>system_spi_n_io_data_1_read</code>	Input	SPI input for data 1.
<code>system_spi_n_io_data_1_write</code>	Output	SPI output for data 1.
<code>system_spi_n_io_data_2_writeEnable</code>	Output	SPI output enable for data 2.
<code>system_spi_n_io_data_2_read</code>	Input	SPI input for data 2.
<code>system_spi_n_io_data_2_write</code>	Output	SPI output for data 2.
<code>system_spi_n_io_data_3_read</code>	Input	SPI input for data 3.
<code>system_spi_n_io_data_3_write</code>	Output	SPI output for data 3.
<code>system_spi_n_io_data_3_writeEnable</code>	Output	SPI output enable for data 3.
<code>system_spi_n_io_ss</code>	Output	SPI SS.

Table 28: SPI Master Register Map

Address Offset	Register Name	Privilege	Width
0x0000_0000	Cmd	Read/Write	32
0x0000_0004	RSP	Read	32
0x0000_0008	Config	Write	32
0x0000_000C	Interrupt	Read/Write	32
0x0000_0020	ClockDivider	Write	32
0x0000_0024	ssSetup	Write	32
0x0000_0028	ssHold	Write	32
0x0000_002C	ssDisable	Write	32
0x0000_0030	ssActiveHigh	Write	32

Cmd Register: 0x0000_0000

31	12	11	10	9	8	7	0
Reserved				SS	RD	WR	data

Bits	Field	Description	Privilege
0-7	data	FIFO data value transmit/receive.	Read/Write
8	WR	Write trigger.	Write
9	RD	Read trigger.	Write
10	Reserved	Reserved.	N/A
11	SS	SPI chip select.	Read/Write
12-31	Reserved	Reserved.	N/A

RSP Register: 0x0000_0004

31	16	15	0
fifoOccupancy		fifoAvailability	

Bits	Field	Description	Privilege
0-15	fifoAvailability	FIFO Availability.	Read
16-32	fifoOccupancy	FIFO Occupancy.	Read

Config Register: 0x0000_0008

31	2	1	0
Reserved			cpha cpol

Bits	Field	Description	Privilege
0	cpol	Clock polarity setting.	Write
1	cpha	Clock phase setting.	Write
2-31	Reserved	Reserved.	N/A

Interrupt Register: 0x0000_000C

31	10	9	8	7	2	1	0
Reserved				rsplnt	cmdlnt	Reserved	
						rsplntEnable	cmdlntEnable

Bits	Field	Description	Privilege
0	cmdlntEnable	Command FIFO empty interrupt enable.	Read/Write
1	rsplntEnable	Read FIFO not empty interrupt enable.	Read/Write
2-7	Reserved	Reserved.	N/A
8	cmdlnt	Command FIFO empty interrupt pending.	Read/Write
9	rsplnt	Read FIFO not empty interrupt pending.	Read/Write
10-31	Reserved	Reserved.	N/A

clockDivider Register: 0x0000_0020

31	clockDivider	0
----	--------------	---

Bits	Field	Description	Privilege
0-31	clockDivider	SPI frequency = FCLK / (2 * clockDivider)	Write

ssSetup Register: 0x0000_0024

31	ssSetup	0
----	---------	---

Bits	Field	Description	Privilege
0-31	ssSetup	Time between the chip select enable and the next byte.	Write

ssHold Register: 0x0000_0028

31	ssHold	0
----	--------	---

Bits	Field	Description	Privilege
0-31	ssHold	Time between the last byte transmission and the chip select disable.	Write

ssDisable Register: 0x0000_002C

31	0
ssDisable	

Bits	Field	Description	Privilege
0-31	ssDisable	Time between the chip select disable and the chip select enable.	Write

ssActiveHigh Register: 0x0000_0030

31	0
ssActiveHigh	

Bits	Field	Description	Privilege
0-31	ssActiveHigh	These bits correspond to the hardware SPI chip select. 0: Chip select is active low. 1: Chip select is active high.	Write

UART Peripheral Interface

The UART peripheral runs at 115200 baud and supports 8 data bits, no parity, and 1 stop bit. The interface starts at these addresses:

- UART 0—0xF801_0000
- UART 1—0xF801_1000

Table 29: UART Ports

Port	Direction	Description
system_uart_0_io_txd	Output	UART 0 transmit.
system_uart_0_io_rxd	Input	UART 0 receive.
system_uart_1_io_txd	Output	UART 1 transmit.
system_uart_1_io_rxd	Input	UART 1 receive.

Control and Status Registers

The following tables show the machine-level CSR implementation.

Table 30: Machine Information Register

Address	Register Name	Privilege	Description	Width
0xF14	mhartid	Read	Hardware thread ID.	32

Table 31: Machine Trap Registers

Address	Register Name	Privilege	Description	Width
0x300	mstatus	Read/Write	Machine status register.	13
0x304	mie	Read/Write	Machine interrupt enable register.	12
0x305	mtvec	Read/Write	Machine trap handler base address.	32

Table 32: Machine Trap Handling Registers

Address	Register Name	Privilege	Description	Width
0x341	mpec	Read/Write	Machine exception program counter.	32
0x342	mcause	Read	Machine trap cause.	32
0x343	mtval	Read	Machine bad address or instruction.	32
0x344	mip	Read/Write	Machine interrupt pending.	12

Machine-Level ISA

Hart ID Register (mhartid): 0xF14

The `mhartid` CSR is a 32-bit read-only register containing the integer ID of the hardware thread running the code. This register must be readable in any implementation. Hart IDs might not necessarily be numbered contiguously in a multiprocessor system, but at least one hart must have a hart ID of zero. Hart IDs must be unique.

31	0
Hart ID	

Bits	Field	Description	Privilege
0-31	Hart ID	Hardware thread ID.	Read

Machine Status Register (*mstatus*): 0x300

The *mstatus* register is a 13-bit read/write register formatted. The *mstatus* register keeps track of and controls the hart's current operating state. Restricted views of the *mstatus* register appear as the *sstatus* and *ustatus* registers in the S-level and U-level ISAs, respectively.

12	11	10	9	8	7	6	5	4	3	2	1	0
MPP	Reserved			MPIE	Reserved			MIE	Reserved			

Bits	Field	Description	Privilege
0-2	Reserved	Reserved.	N/A
3	MIE	Machine interrupt enable register.	Read/Write
4-6	Reserved	Reserved.	N/A
7	MPIE	Machine previous interrupt enable.	Read/Write
8-10	Reserved	Reserved.	N/A
11-12	MPP	Machine Previous privilege mode.	Read/Write

Machine Trap-Vector Base-Address Register (*mtvec*): 0x305

The *mtvec* register is a 32-bit read/write register that holds trap vector configuration, consisting of a vector base address (*base*) and a vector mode (*mode*).

31											2	1	0
base											mode		

Bits	Field	Description	Privilege
0-1	mode	Vector mode. 0: Direct. All exceptions set pc to BASE 1: Vectored. Asynchronous interrupts set pc to BASE + 4xcause ≥ 2: Reserved	Read/Write
2-31	base	Vector base address.	Read/Write

Machine Interrupt Enable Register (*mie*): 0x304

The *mie* register is a 12-bit read/write register containing interrupt enable bits.

11	10	9	8	7	6	5	4	3	2	1	0
MEIE	Reserved			MTIE	Reserved			MSIE	Reserved		

Bits	Field	Description	Privilege
0-2	Reserved	Reserved.	N/A
3	MSIE	Machine software interrupt enable.	Read/Write
4-6	Reserved	Reserved.	N/A
7	MTIE	Machine timer interrupt enable.	Read
8-10	Reserved	Reserved.	N/A
11	MEIE	Machine external interrupt enable.	Read

Machine Exception Program Counter (*mepc*): 0x341

mepc is a 32-bit read/write register. The low bit of *mepc* (*mepc*[0]) is always zero. On implementations that support only *IALIGN*=32, the two low bits (*mepc*[1:0]) are always zero.

31	0
<i>mepc</i>	

Bits	Field	Description	Privilege
0-31	<i>mepc</i>	Machine exception program counter.	Read/Write

Machine Cause Register (*mcause*): 0x342

The *mcause* register is a 32-bit read-write register. When a trap is taken into M-mode, *mcause* is written with a code indicating the event that caused the trap. Otherwise, *mcause* is never written by the implementation, though it may be explicitly written by software.

31	30	0
Interrupt	Exception Code	

Bits	Field	Description	Privilege
0-30	Exception code	See Table 33: Machine Cause Register (<i>mcause</i>) Values after Trap on page 30.	Read
31	Interrupt	<i>mcause</i> interrupt bit.	Read

Table 33: Machine Cause Register (*mcause*) Values after Trap

Interrupt	Exception Code	Description
1	0	Reserved.
1	1	Supervisor software interrupt.
1	2	Reserved.
1	3	Machine software interrupt.
1	4	User timer interrupt.
1	5	Supervisor timer interrupt.
1	6	Reserved.
1	7	Machine timer interrupt.
1	8	User external interrupt.
1	9	Supervisor external interrupt.
1	10	Reserved.
1	11	Machine external interrupt.
1	≥12	Reserved.
0	0	Instruction address misaligned.
0	1	Instruction access fault.
0	2	Illegal instruction.
0	3	Breakpoint.

Interrupt	Exception Code	Description
0	4	Load address misaligned.
0	5	Load access fault.
0	6	Store/AMO address misaligned.
0	7	Store/AMO access fault.
0	8	Reserved.
0	9	Reserved.
0	10	Reserved.
0	11	Environment call from M-mode.
0	12	Instruction page fault.
0	13	Load page fault.
0	14	Reserved.
0	15	Store/AMO page fault.
0	≥16	Reserved.

Machine Trap Value Register (mtval): 0x343

The `mtval` register is a 32-bit register. When a trap is taken into M-mode, `mtval` is either set to zero or written with exception-specific information to assist software in handling the trap. Otherwise, `mtval` is never written by the implementation, though it may be explicitly written by software. The hardware platform will specify which exceptions must set `mtval` informatively and which may unconditionally set it to zero.

31	0
mtval	

Bits	Field	Description	Privilege
0-31	mtval	Machine trap value register bit.	Read/Write

Machine Interrupt Pending Register (mip): 0x344

The `mip` register is a 12-bit read/write register containing information on pending interrupts.

11	10	9	8	7	6	5	4	3	2	1	0
MEIP	Reserved			MTIP	Reserved			MSIP	Reserved		

Bits	Field	Description	Privilege
0-2	Reserved	Reserved.	N/A
3	MSIP	Machine software interrupt pending.	Read/Write
4-6	Reserved	Reserved.	N/A
7	MTIP	Machine timer interrupt pending.	Read
8-10	Reserved	Reserved.	N/A
11	MEIP	Machine external interrupt pending.	Read

Revision History

Table 34: Revision History

Date	Version	Description
June 2020	1.0	Initial release.