Jade RISC-V SoC Data Sheet

DS-JADE-v1.0
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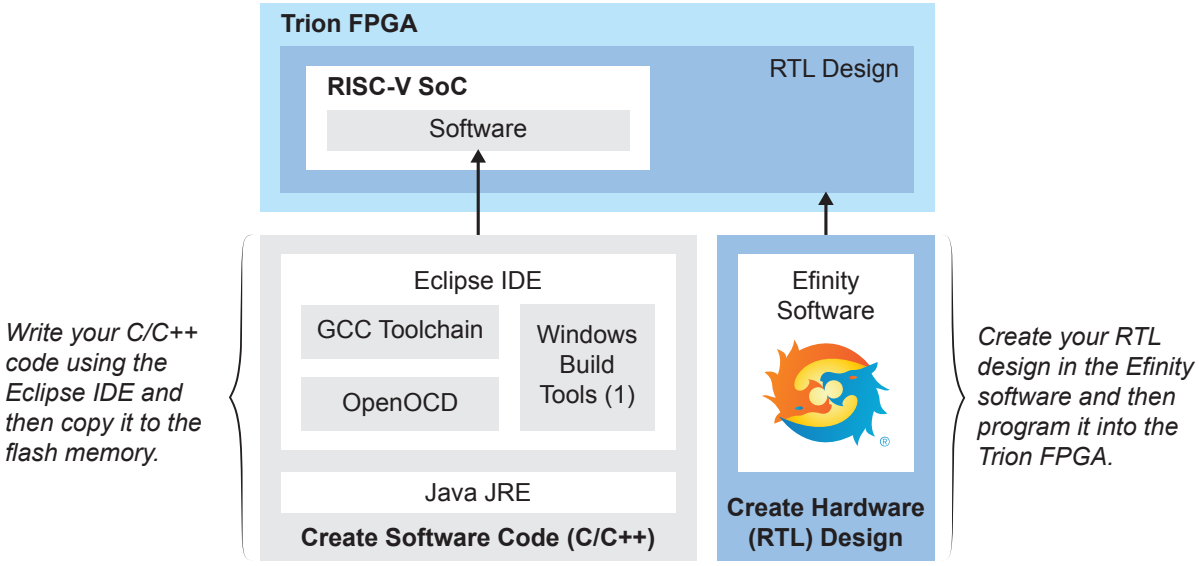
www.efinixinc.com

Contents

Introduction

Efinix provides the light-weight, cached soft RISC-V SoC, Jade, that blends performance with a smaller footprint. This SoC is ideal for general-purpose applications that use triple-speed Ethernet and communications protocols, such as command and control, industrial automation, or data logging systems. Some example applications for the Jade SoC are large LED billboards and industrial controllers. This core is similar to the open-source SaxonSOC, but it has been optimized for Trion® FPGAs.

Figure 1: Jade RISC-V SoC Design Flow



1. Windows build tools required on Windows platforms only.

Learn more: For details on developing RTL designs or creating software, refer to the Jade RISC-V Hardware and Software User Guide.

VexRiscv RISC-V Core

The Jade SoC is based on the VexRiscv core created by Charles Papon. The VexRiscv core is a 32-bit CPU using the ISA RISCV32I with M and C extensions, has five pipeline stages (fetch, decode, execute, memory, and writeback), and a configurable feature set. In the Jade SoC, the VexRiscv core supports an APB3 bus interface, has instruction and data caches, and can run at speeds up to 1.2 DMIPS/MHz.

The VexRiscv core won first place in the RISC-V SoftCPU contest in 2018.(1)

(1) https://www.businesswire.com/news/home/20181206005747/en/RISC-V-SoftCPU-Contest-Winners-Demonstrate-Cutting-Edge-RISC-V

Features

- VexRiscv processor with 5 pipeline stages (fetch, decode, execute, memory, and write back), interrupts and exception handling with machine mode
  - 4 KB data cache
  - 4 KB instruction cache
- 50 MHz system clock frequency
- 32 KB on-chip RAM with boot loader for SPI flash
- APB3 peripherals:
  - 16 GPIOs
  - 2 I^2C masters and slaves
  - Machine timer
  - PLIC
  - 2 SPI flash masters with a maximum clock frequency of 25 MHz
  - 1 UART with 115,200 baud rate
  - 1 slave user peripheral

FPGA Support

The Jade SoC supports T20, T35, T55, T85, and T120 Trion® FPGAs.

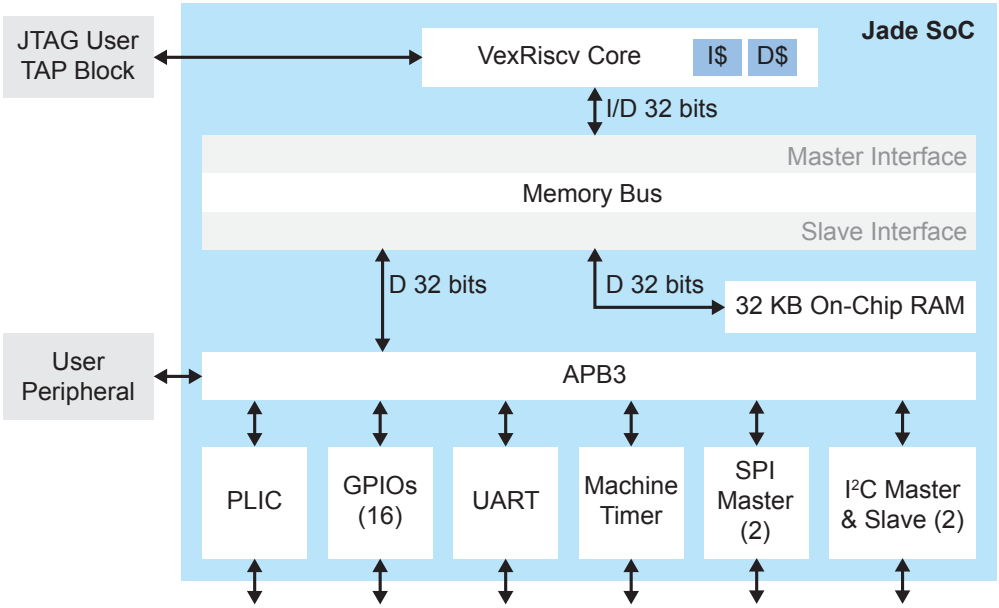
Resource Utilization and Performance

FPGA	Logic Utilization (LUTs)	Memory Blocks	f_{MAX} (MHz)	Language	Efinity Version
T20 BGA256 C4	6,465	93	SoC: 69.636	Verilog HDL	2019.3

Functional Description

The Jade SoC incorporates a 32-bit RISC-V processor, 4 KB instruction cache, 4 KB data cache, 32 KB of on-chip RAM, and a variety of peripherals (including 1 APB3 slave peripherals).

Figure 2: Jade SoC Block Diagram



Address Map

Table 1: Default Address Map, Interrupt ID, and Cached Channels

Device	Address	Size	Interrupt ID	Region
Null	0x0000_0FFF - 0x0000_0000	4K	–	–
GPIO	0xF800_0FFF – 0xF800_0000	4K	[0]: 12 [1]: 13	I/O
I^2C 0	0xF801_8FFF – 0xF801_8000	4K	8	I/O
I^2C 1	0xF801_9FFF – 0xF801_9000	4K	9	I/O
Machine timer	0xF800_8FFF – 0xF800_8000	4K	31	I/O
PLIC	0xF8C0_0FFF - 0xF8C0_0000	4K	–	I/O
SPI master 0	0xF801_4FFF – 0xF801_4000	4K	4	I/O
SPI master 1	0xF801_5FFF – 0xF801_5000	4K	5	I/O
UART	0xF801_0FFF – 0xF801_0000	4K	1	I/O
User peripheral	0xF880_0FFF – 0xF880_0000	4K	–	I/O
On-chip BRAM	0xF900_7FFF – 0xF900_0000	32K	–	Cache
External interrupt	-	-	25	I/O

Note: The RISC-V GCC compiler does not support user address spaces starting at 0x0000_0000.

Flash Address

When the FPGA boots up, the Jade SoC copies your binary application file from a SPI flash device to the on-chip memory, and then begins execution.

The SPI flash binary address starts at 0x0038_0000.

Clocks

Table 2: Clock Ports

Port	Direction	Description
io_systemClock	Input	Provides a 50 MHz clock for the SoC.

Interrupts

Table 3: Interrupt Ports

Port	Direction	Description
userInterruptA	Input	Provides an external interrupt.

Resets

The Jade SoC has as master reset signal, `io_asyncReset` that triggers a system reset. Your RTL design should hold `io_asyncReset` for 10 ns to reset the whole SoC system completely. When you assert `io_asyncReset`, the SoC asserts:

- `io_systemReset`, which resets the RISC-V processor, on-chip memory, and peripherals

Once `io_systemReset` goes low, the user binary code is executed.

Table 4: Reset Ports

Port	Direction	Description
io_asyncReset	Input	Active-high asynchronous reset for the entire system.
io_systemReset	Output	Synchronous active-high reset for systemClk.

APB3 Interface

The following table shows the ports for the APB3 user slave peripheral. Refer to the AMBA APB Protocol Specification for APB port descriptions and handshake information.

Table 5: APB3 Ports

Port	Direction	Description
io_apbSlave_0_PADDR[11:0]	Output	User address.
io_apbSlave_0_PSEL	Output	User select.
io_apbSlave_0_PENABLE	Output	User enable.
io_apbSlave_0_PREADY	Input	User ready.
io_apbSlave_0_PWRITE	Output	User direction.
io_apbSlave_0_PWDATA[31:0]	Output	User write data.
io_apbSlave_0_PRDATA[31:0]	Input	User read data.
io_apbSlave_0_PSLVERROR	Input	User transfer failure.

JTAG Interface

The Jade SoC uses the JTAG User TAP interface block to communicate with the OpenOCD debugger.

Table 6: JTAG Ports

Port	Direction	Description
jtagCtrl_enable	Input	Indicates that the user instruction is active for the interface.
tagCtrl_capture	Input	TAP controller is in the capture state.
jtagCtrl_shift	Input	TAP controller is in the shift state.
jtagCtrl_update	Input	TAP controller in the update state.
jtagCtrl_reset	Input	TAP controller is in the reset state.
jtagCtrl_tdi	Input	JTAG TDI for debugging.
jtagCtrl_tdo	Output	JTAG TDO for debugging.
jtagCtrl_tck	Input	JTAG TCK for debugging.

GPIO Peripheral Interface

The GPIO interface starts at address 0xF800_0000.

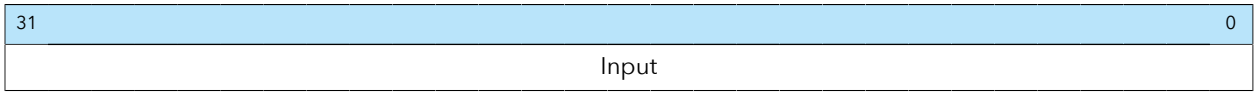
Table 7: GPIO Ports

Port	Direction	Description
system_gpio_0_io_read[15:0]	Input	GPIO input.
system_gpio_0_io_write[15:0]	Output	GPIO output.
system_gpio_0_io_writeEnable[15:0]	Output	GPIO output enable.

Table 8: GPIO Register Map

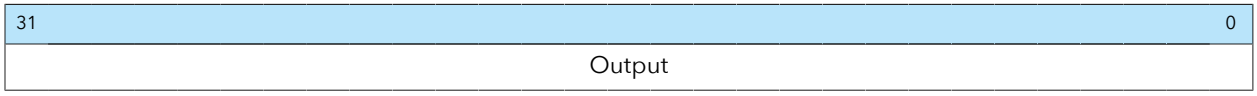
Address Offset	Register Name	Privilege	Width
0x0000_0000	Input	Read/Write	32
0x0000_0004	Output	Read/Write	32
0x0000_0008	Output Enable	Read/Write	32
0x0000_0020	Interrupt Rise Enable	Read/Write	32
0x0000_0024	Interrupt Fall Enable	Read/Write	32
0x0000_0028	Interrupt High Enable	Read/Write	32
0x0000_002C	Interrupt Low Enable	Read/Write	32

Input Register: 0x0000_0000



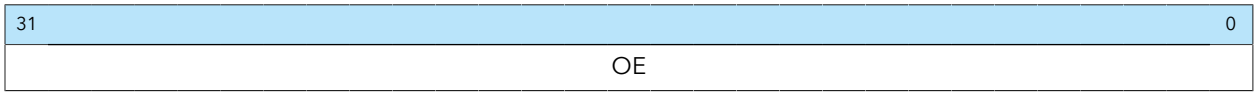
Bits	Field	Description	Privilege
0-31	Input	Set GPIO pin as an input (32 pins).	Read/Write

Output Register: 0x0000_0004



Bits	Field	Description	Privilege
0-31	Output	Set GPIO pin as an output (32 pins).	Read/Write

Output Enable Register: 0x0000_0008



Bits	Field	Description	Privilege
0-31	OE	Enable GPIO output pin (32 pins).	Read/Write

Interrupt Rise Enable Register: 0x0000_0020

31	0
IntRiseEn	

Bits	Field	Description	Privilege
0-31	IntRiseEn	Enable a rise interrupt on the GPIO pin (32 pins).	Read/Write

Interrupt Fall Enable Register: 0x0000_0024

31	0
IntFallEn	

Bits	Field	Description	Privilege
0-31	IntFallEn	Enable a fall interrupt on the GPIO pin (32 pins).	Read/Write

Interrupt High Enable Register: 0x0000_0028

31	0
IntHighEn	

Bits	Field	Description	Privilege
0-31	IntHighEn	Enable a high interrupt on the GPIO pin (32 pins).	Read/Write

Interrupt Low Enable Register: 0x0000_002C

31	0
IntLowEn	

Bits	Field	Description	Privilege
0-31	IntLowEn	Enable a low interrupt on the GPIO pin (32 pins).	Read/Write

I²C Peripheral Interface

The Jade SoC has 2 I²C master/slave peripherals. The I²C interface starts at these addresses:

- I²C 0—0xF801_8000
- I²C 1—0xF801_9000

Table 9: I²C Peripheral Ports (User)

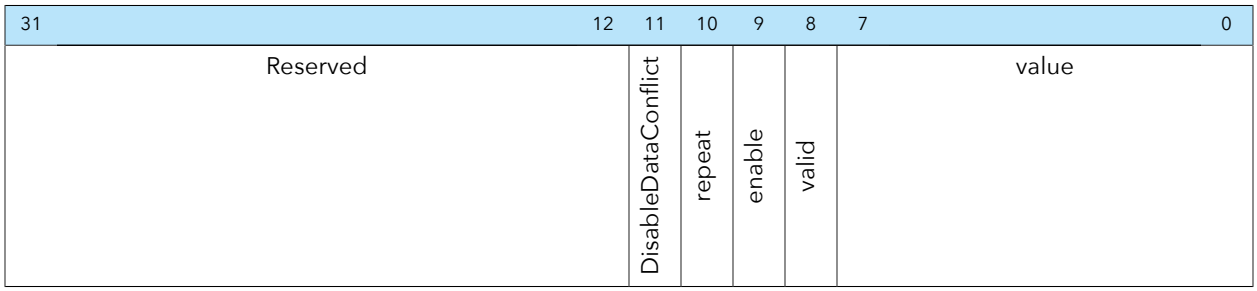
Where *n* is 0 or 1

Port	Direction	Description
system_i2c_*n*_io_sda_write	Output	SDA output for user device.
system_i2c_*n*_io_sda_read	Input	SDA input for user device.
system_i2c_*n*_io_scl_write	Output	SCL output for user device.
system_i2c_*n*_io_scl_read	Input	SCL input for user device.

Table 10: I²C Register Map

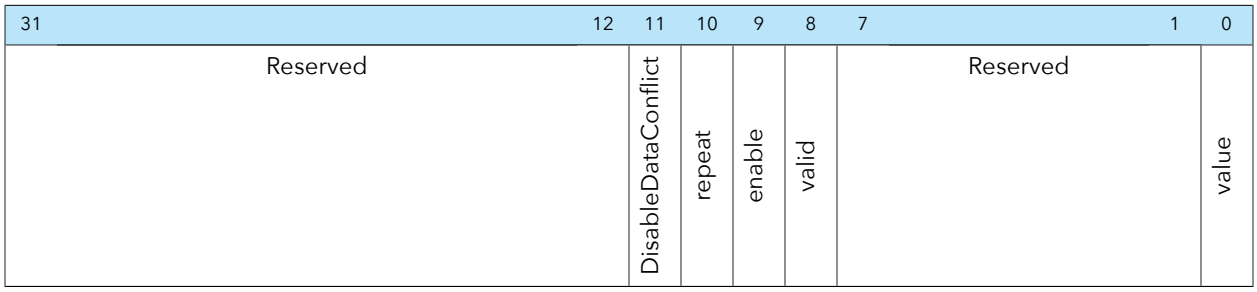
Address Offset	Register Name	Privilege	Width
0x0000_0000	txData	Read/Write	32
0x0000_0004	txAck	Read/Write	32
0x0000_0008	rxData	Read/Write	32
0x0000_000C	rxAck	Read/Write	32
0x0000_0020	Interrupt	Read/Write	32
0x0000_0024	Interrupt Clears	Read/Write	32
0x0000_0028	Sampling Clock Divider	Read/Write	32
0x0000_002C	Timeout	Write	32
0x0000_0030	tsuData	Write	32
0x0000_0040	Master Status	Read/Write	32
0x0000_0050	tlow	Read/Write	32
0x0000_0054	tHigh	Read/Write	32
0x0000_0058	tBuf	Read/Write	32
0x0000_0080	Filtering Status	Read/Write	32
0x0000_0084	Hit Context	Read/Write	32
0x0000_0088	Filtering Configuration	Read/Write	32

txData Register: 0x0000_0000



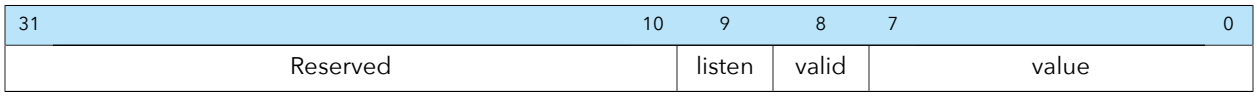
Bits	Field	Description	Privilege
0-7	value	Transmit data value.	Write
8	valid	Transmit data valid bit.	Read/Write
9	enable	Transmit data enable.	Read/Write
10	repeat	Transmit data repeat bit.	Write
11	DisableDataConflict	Disable transmit data conflict.	Write
12-31	Reserved	Reserved.	N/A

txAck Register: 0x0000_0004



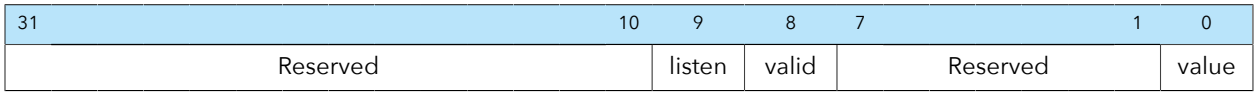
Bits	Field	Description	Privilege
0	value	Transmit acknowledge bit.	Write
1-7	Reserved	Reserved.	N/A
8	valid	Transmit acknowledge valid bit.	Read/Write
9	enable	Transmit acknowledge enable.	Read/Write
10	repeat	Transmit acknowledge repeat bit.	Write
11	DisableDataConflict	Disable transmit acknowledge conflict.	Write
12-31	Reserved	Reserved.	N/A

rxData Register: 0x0000_0008



Bits	Field	Description	Privilege
0-7	value	Received data.	Read
8	valid	Receive data valid.	Read
9	listen	Start listen data.	Write
10-31	Reserved	Reserved.	N/A

rxAck Register: 0x0000_000C



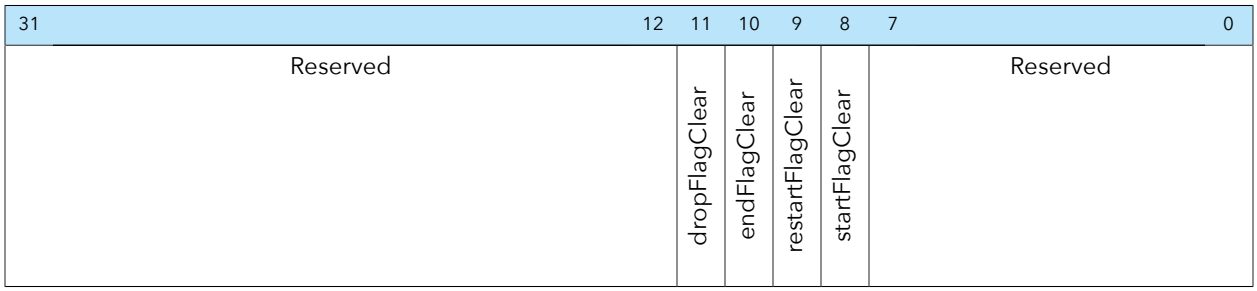
Bits	Field	Description	Privilege
0	value	Received acknowledge.	Read
1-7	Reserved	Reserved.	N/A
8	valid	Receive acknowledge valid.	Read
9	listen	Start listen acknowledge.	Write
10-31	Reserved	Reserved.	N/A

Interrupt Register: 0x0000_0020

31 22	21	20	19 18	17	16	15 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	filterFlag	clockGenBusyFlag	Reserved	filterEnable	clockGenBusyEnable	Reserved	dropFlag	endFlag	restartFlag	startFlag	dropEnable	endEnable	restartEnable	startEnable	txAckEnable	txDataEnable	rxAckEnable	rxDataEnable

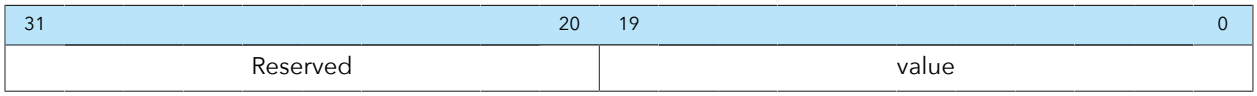
Bits	Field	Description	Privilege
0	rxDataEnable	Receive data interrupt enable	Read/Write
1	rxAckEnable	Receive acknowledge interrupt enable	Read/Write
2	txDataEnable	Transmit data interrupt enable	Read/Write
3	txAckEnable	Transmit acknowledge interrupt enable	Read/Write
4	startEnable	Start interrupt enable	Read/Write
5	restartEnable	Restart interrupt enable	Read/Write
6	endEnable	End interrupt enable	Read/Write
7	dropEnable	Drop interrupt enable	Read/Write
8	startFlag	Start interrupt flag	Read
9	restartFlag	Restart interrupt flag	Read
10	endFlag	End interrupt flag	Read
11	dropFlag	Drop interrupt flag	Read
12-15	Reserved	Reserved.	N/A
16	clockGenBusyEnable	Master clock generation interrupt enable.	Read/Write
17	filterEnable	Slave address filtering hit interrupt enable	Read/Write
18-19	Reserved	Reserved.	N/A
20	clockGenBusyFlag	Master clock generation interrupt flag.	Read
21	filterFlag	Slave address filtering hit interrupt flag.	Read
22-31	Reserved	Reserved.	N/A

Interrupt Clears Register: 0x0000_0024



Bits	Field	Description	Privilege
0-7	Reserved	Reserved.	N/A
8	startFlagClear	Clear start flag.	Write
9	restartFlagClear	Clear restart flag.	Write
10	endFlagClear	Clear end flag.	Write
10	dropFlagClear	Clear drop flag.	Write
12-31	Reserved	Reserved.	N/A

Timeout Register: 0x0000_002C

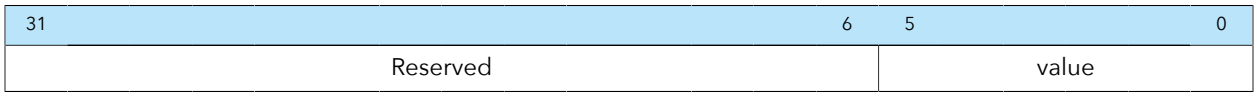


Bits	Field	Description	Privilege
0-19	value	Inactive timeout setting.	Write
20-31	Reserved	Reserved.	N/A

Sampling Clock Divider Register: 0x0000_0028

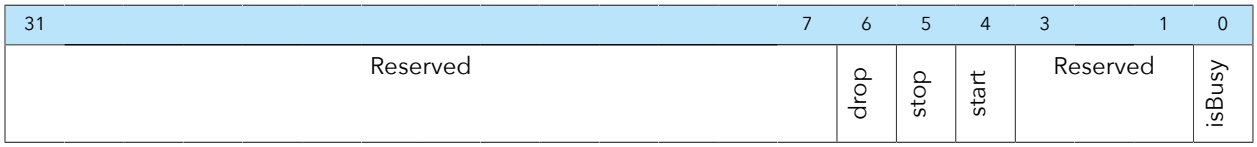
Bits	Field	Description	Privilege
0-9	samplingClockDividerWidth	Clock divider width. Controls the rate at which the I^2C controller reads SCL and SDA.	Read/Write
10-31	Reserved	Reserved.	N/A

tsuData Register: 0x0000_0030



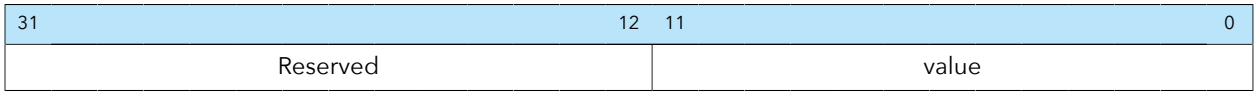
Bits	Field	Description	Privilege
0-5	value	Data setup time.	Write
6-31	Reserved	Reserved.	N/A

Master Status Register: 0x0000_0040



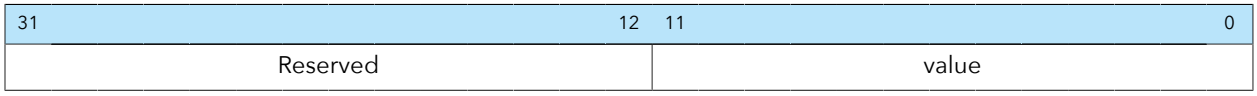
Bits	Field	Description	Privilege
0	isBusy	Master busy.	Read
1-3	Reserved	Reserved.	N/A
4	start	Master start.	Read/Write
5	stop	Master stop.	Read/Write
6	drop	Master drop.	Read/Write
6-31	Reserved	Reserved.	N/A

tLow Register: 0x0000_0050



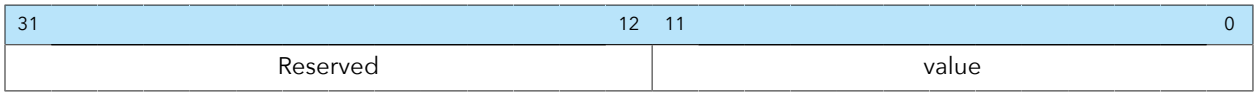
Bits	Field	Description	Privilege
0-11	value	SCL low period.	Write
12-31	Reserved	Reserved.	N/A

tHigh Register: 0x0000_0054



Bits	Field	Description	Privilege
0-11	value	SCL high period.	Write
12-31	Reserved	Reserved.	N/A

tBuf Register: 0x0000_0058



Bits	Field	Description	Privilege
0-11	value	Start and stop bus free time.	Write
12-31	Reserved	Reserved.	N/A

Filtering Status Register: 0x0000_0080

31 … 8	7	6	5	4	3	2	1	0
Reserved	hit_7	hit_6	hit_5	hit_4	hit_3	hit_2	hit_1	hit_0

Bits	Field	Description	Privilege
0	hit_0	Filtering hit bit 0.	Read
1	hit_1	Filtering hit bit 1.	Read
2	hit_2	Filtering hit bit 2.	Read
3	hit_3	Filtering hit bit 3.	Read
4	hit_4	Filtering hit bit 4.	Read
5	hit_5	Filtering hit bit 5.	Read
6	hit_6	Filtering hit bit 6.	Read
7	hit_7	Filtering hit bit 7.	Read
8-32	Reserved	Reserved.	N/A

Hit Context Register: 0x0000_0084

31 … 1	0
Reserved	rw

Bits	Field	Description	Privilege
0	rw	Hit context read.	Read
1-31	Reserved	Reserved.	N/A

PLIC Peripheral Interface

The PLIC interface starts at address 0xF8C0_0000.

Table 11: RISC-V PLIC Operation Parameters

Defines	Description
Interrupt priorities registers	The interrupt priority for each interrupt source.
Interrupt pending bits registers	The interrupt pending status of each interrupt source.
Interrupt enables registers	Enables the interrupt source of each context.
Priority thresholds registers	The interrupt priority threshold of each context.
Interrupt claim registers	The register to acquire interrupt source ID of each context.
Interrupt completion registers	The register to send interrupt completion message to the associated gateway.

SPI Master Peripheral Interface

The SPI master peripheral interface supports traditional 4-wire SPI as well as quad-SPI mode, which sends 4 data bits per clock cycle. When implementing the SPI peripheral in traditional dual-line mode, use the `data_0` ports as MOSI and and the `data_1` ports as MISO.

The SPI master interface starts at address:

- SPI master 0—0xF801_4000
- SPI master 1—0xF801_5000

Table 12: SPI Master Ports

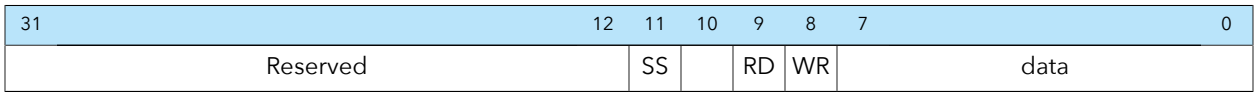
Where *n* is 0 or 1

Port	Direction	Description
system_spi_*n*_io_sclk_write	Output	SPI SCK.
system_spi_*n*_io_data_0_writeEnable	Output	SPI output enable for data 0.
system_spi_*n*_io_data_0_read	Input	SPI input for data 0.
system_spi_*n*_io_data_0_write	Output	SPI output for data 0.
system_spi_*n*_io_data_1_writeEnable	Output	SPI output enable for data 1.
system_spi_*n*_io_data_1_read	Input	SPI input for data 1.
system_spi_*n*_io_data_1_write	Output	SPI output for data 1.
system_spi_*n*_io_data_2_writeEnable	Output	SPI output enable for data 2.
system_spi_*n*_io_data_2_read	Input	SPI input for data 2.
system_spi_*n*_io_data_2_write	Output	SPI output for data 2.
system_spi_*n*_io_data_3_read	Input	SPI input for data 3.
system_spi_*n*_io_data_3_write	Output	SPI output for data 3.
system_spi_*n*_io_data_3_writeEnable	Output	SPI output enable for data 3.
system_spi_*n*_io_ss	Output	SPI SS.

Table 13: SPI Master Register Map

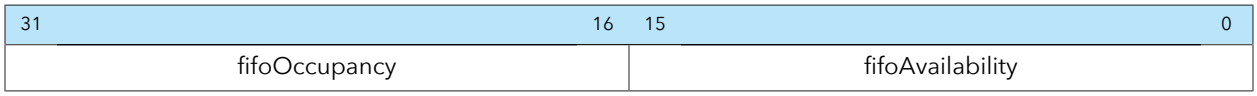
Address Offset	Register Name	Privilege	Width
0x0000_0000	Cmd	Read/Write	32
0x0000_0004	RSP	Read	32
0x0000_0008	Config	Write	32
0x0000_000C	Interrupt	Read/Write	32
0x0000_0020	ClockDivider	Write	32
0x0000_0024	ssSetup	Write	32
0x0000_0028	ssHold	Write	32
0x0000_002C	ssDisable	Write	32
0x0000_0030	ssActiveHigh	Write	32

Cmd Register: 0x0000_0000



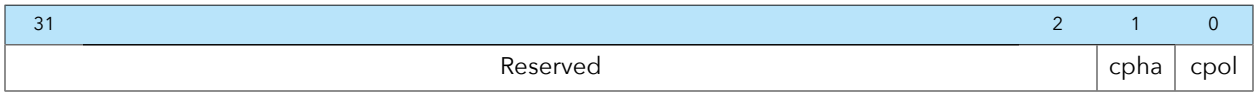
Bits	Field	Description	Privilege
0-7	data	FIFO data value transmit/receive.	Read/Write
8	WR	Write trigger.	Write
9	RD	Read trigger.	Write
10	Reserved	Reserved.	N/A
11	SS	SPI chip select.	Read/Write
12-31	Reserved	Reserved.	N/A

RSP Register: 0x0000_0004



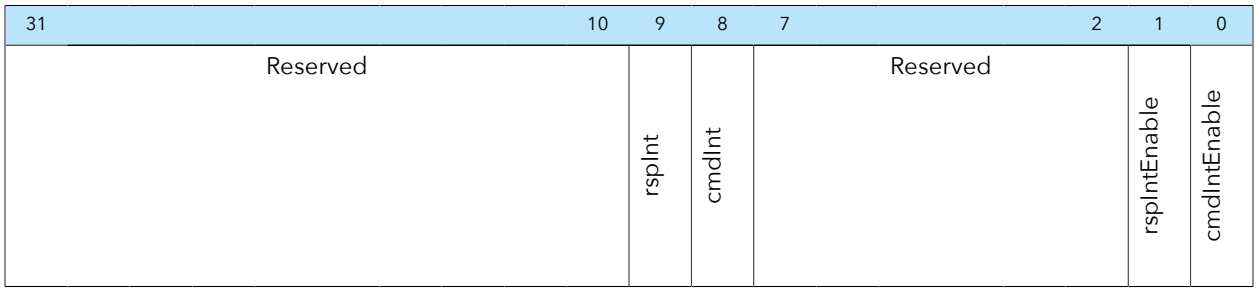
Bits	Field	Description	Privilege
0-15	fifoAvailability	FIFO Availability.	Read
16-32	fifoOccupancy	FIFO Occupancy.	Read

Config Register: 0x0000_0008



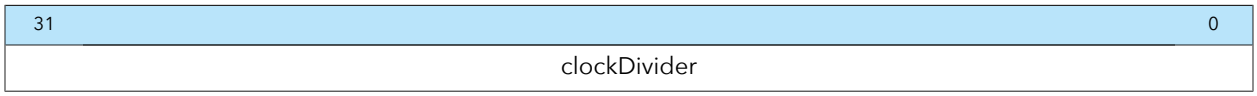
Bits	Field	Description	Privilege
0	cpol	Clock polarity setting.	Write
1	cpha	Clock phase setting.	Write
2-31	Reserved	Reserved.	N/A

Interrupt Register: 0x0000_000C



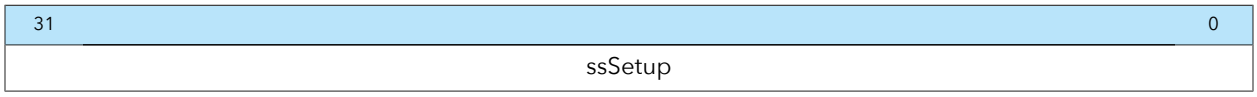
Bits	Field	Description	Privilege
0	cmdIntEnable	Command FIFO empty interrupt enable.	Read/Write
1	rspIntEnable	Read FIFO not empty interrupt enable.	Read/Write
2-7	Reserved	Reserved.	N/A
8	cmdInt	Command FIFO empty interrupt pending.	Read/Write
9	rspInt	Read FIFO not empty interrupt pending.	Read/Write
10-31	Reserved	Reserved.	N/A

clockDivider Register: 0x0000_0020



Bits	Field	Description	Privilege
0-31	clockDivider	SPI frequency = FCLK / (2 * clockDivider)	Write

ssSetup Register: 0x0000_0024



Bits	Field	Description	Privilege
0-31	ssSetup	Time between the chip select enable and the next byte.	Write

ssHold Register: 0x0000_0028

Bits	Field	Description	Privilege
0-31	ssHold	Time between the last byte transmission and the chip select disable.	Write

ssDisable Register: 0x0000_002C

31	0
ssDisable	

Bits	Field	Description	Privilege
0-31	ssDisable	Time between the chip select disable and the chip select enable.	Write

ssActiveHigh Register: 0x0000_0030

31	0
ssActiveHigh	

Bits	Field	Description	Privilege
0-31	ssActiveHigh	These bits correspond to the hardware SPI chip select. 0: Chip select is active low. 1: Chip select is active high.	Write

UART Peripheral Interface

The UART peripheral runs at 115200 baud and supports 8 data bits, no partiy, and 1 stop bit. The interface starts at address 0xF801_0000.

Table 14: UART Ports

Port	Direction	Description
system_uart_0_io_txd	Output	UART 0 transmit.
system_uart_0_io_rxd	Input	UART 0 receive.

Control and Status Registers

The following tables show the machine-level CSR implementation.

Table 15: Machine Information Register

Address	Register Name	Privilege	Description	Width
0xF14	mhartid	Read	Hardware thread ID.	32

Table 16: Machine Trap Registers

Address	Register Name	Privilege	Description	Width
0x300	mstatus	Read/Write	Machine status register.	13
0x304	mie	Read/Write	Machine interrupt enable register.	12
0x305	mtvec	Read/Write	Machine trap handler base address.	32

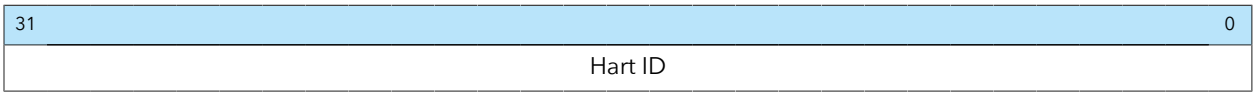
Table 17: Machine Trap Handling Registers

Address	Register Name	Privilege	Description	Width
0x341	mpec	Read/Write	Machine exception program counter.	32
0x342	mcause	Read	Machine trap cause.	32
0x343	mtval	Read	Machine bad address or instruction.	32
0x344	mip	Read/Write	Machine interrupt pending.	12

Machine-Level ISA

Hart ID Register (mhartid): 0xF14

The `mhartid` CSR is a 32-bit read-only register containing the integer ID of the hardware thread running the code. This register must be readable in any implementation. Hart IDs might not necessarily be numbered contiguously in a multiprocessor system, but at least one hart must have a hart ID of zero. Hart IDs must be unique.



Bits	Field	Description	Privilege
0-31	Hart ID	Hardware thread ID.	Read

Machine Status Register (mstatus): 0x300

The `mstatus` register is a 13-bits read/write register formatted. The `mstatus` register keeps track of and controls the hart's current operating state. Restricted views of the `mstatus` register appear as the `sstatus` and `ustatus` registers in the S-level and U-level ISAs, respectively.

12	11	10	9	8	7	6	5	4	3	2	1	0
MPP		Reserved			MPIE	Reserved			MIE	Reserved		

Bits	Field	Description	Privilege
0-2	Reserved	Reserved.	N/A
3	MIE	Machine interrupt enable register.	Read/Write
4-6	Reserved	Reserved.	N/A
7	MPIE	Machine previous interrupt enable.	Read/Write
8-10	Reserved	Reserved.	N/A
11-12	MPP	Machine Previous privilege mode.	Read/Write

Machine Trap-Vector Base-Address Register (mtvec): 0x305

The `mtvec` register is a 32-bit read/write register that holds trap vector configuration, consisting of a vector base address (base) and a vector mode (mode).

31	2	1	0
base		mode	

Bits	Field	Description	Privilege
0-1	mode	Vector mode. 0: Direct. All exceptions set pc to BASE 1: Vectored. Asynchronous interrupts set pc to BASE + 4xcause ≥ 2: Reserved	Read/Write
2-31	base	Vector base address.	Read/Write

Machine Interrupt Enable Register (mie): 0x304

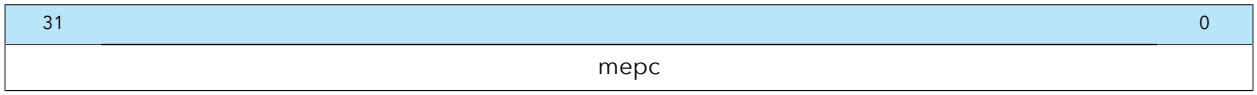
The `mie` register is a 12-bit read/write register containing interrupt enable bits.

11	10	9	8	7	6	5	4	3	2	1	0
MEIE	Reserved			MTIE	Reserved			MSIE	Reserved		

Bits	Field	Description	Privilege
0-2	Reserved	Reserved.	N/A
3	MSIE	Machine software interrupt enable.	Read/Write
4-6	Reserved	Reserved.	N/A
7	MTIE	Machine timer interrupt enable.	Read
8-10	Reserved	Reserved.	N/A
11	MEIE	Machine external interrupt enable.	Read

Machine Exception Program Counter (mepc): 0x341

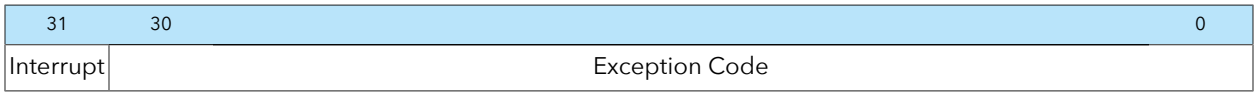
`mepc`is a 32-bit read/write register. The low bit of `mepc` (`mepc[0]`) is always zero. On implementations that support only IALIGN=32, the two low bits (`mepc[1:0]`) are always zero.



Bits	Field	Description	Privilege
0-31	mepc	Machine exception program counter.	Read/Write

Machine Cause Register (mcause): 0x342

The `mcause` register is a 32-bit read-write register. When a trap is taken into M-mode, `mcause` is written with a code indicating the event that caused the trap. Otherwise, `mcause` is never written by the implementation, though it may be explicitly written by software.



Bits	Field	Description	Privilege
0-30	Exception code	See **Table 18: Machine Cause Register (mcause) Values after Trap** on page 25.	Read
31	Interrupt	mcause interrupt bit.	Read

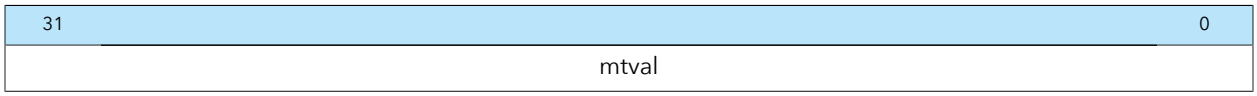
Table 18: Machine Cause Register (mcause) Values after Trap

Interrupt	Exception Code	Description
1	0	Reserved.
1	1	Supervisor software interrupt.
1	2	Reserved.
1	3	Machine software interrupt.
1	4	User timer interrupt.
1	5	Supervisor timer interrupt.
1	6	Reserved.
1	7	Machine timer interrupt.
1	8	User external interrupt.
1	9	Supervisor external interrupt.
1	10	Reserved.
1	11	Machine external interrupt.
1	≥12	Reserved.
0	0	Instruction address misaligned.
0	1	Instruction access fault.
0	2	Illegal instruction.
0	3	Breakpoint.

Interrupt	Exception Code	Description
0	4	Load address misaligned.
0	5	Load access fault.
0	6	Store/AMO address misaligned.
0	7	Store/AMO access fault.
0	8	Reserved.
0	9	Reserved.
0	10	Reserved.
0	11	Environment call from M-mode.
0	12	Instruction page fault.
0	13	Load page fault.
0	14	Reserved.
0	15	Store/AMO page fault.
0	≥16	Reserved.

Machine Trap Value Register (mtval): 0x343

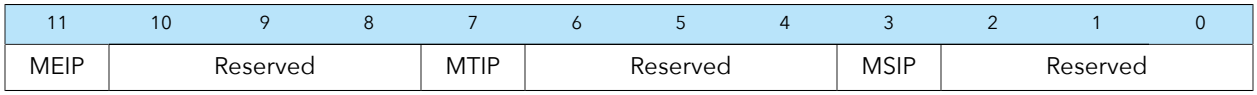
The `mtval` register is a 32-bit register. When a trap is taken into M-mode, `mtval` is either set to zero or written with exception-specific information to assist software in handling the trap. Otherwise, `mtval` is never written by the implementation, though it may be explicitly written by software. The hardware platform will specify which excep-tions must set `mtval` informatively and which may unconditionally set it to zero.



Bits	Field	Description	Privilege
0-31	mtval	Machine trap value register bit.	Read/Write

Machine Interrupt Pending Register (mip): 0x344

The `mip` register is a 12-bit read/write register containing information on pending interrupts.



Bits	Field	Description	Privilege
0-2	Reserved	Reserved.	N/A
3	MSIP	Machine software interrupt pending.	Read/Write
4-6	Reserved	Reserved.	N/A
7	MTIP	Machine timer interrupt pending.	Read
8-10	Reserved	Reserved.	N/A
11	MEIP	Machine external interrupt pending.	Read

Revision History

Table 19: Revision History

Date	Version	Description
June 2020	1.0	Initial release.