# AN 070: Understanding SPI Flash Operations in SIP Devices

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# Contents

# Introduction

Efinix® provides some FPGAs as SIPs, in which the FPGA is combined with another device, such as flash memory. SIPs that include flash memory make it easy for you to integrate the FPGA on your board because you do not need to include a flash device. Instead, the FPGA configures itself from the flash memory in the package. This application note explains how to use the flash device for SIPs.

# SPI Flash Block Interface Features

The T20 and Ti60 comes with 2 MB of SPI flash. The following table outlines the signal connection between the SPI flash interface and FPGA fabric.

*Table 1: Interface Mapping*

| SPI Name | FPGA Pin | Interface to FPGA Fabric | | | | |
|---|---|---|---|---|---|---|
| | | x1 Mode (default) | x2 Mode | x4 Mode | Fabric Signal | Fabric Direction |
| SPI_CS_N | SSL_N | Input | Input | Input | CS_N_OUT | Input |
| | | | | | CS_N_OE | Input |
| SPI_SCLK | CCK | Input | Input | Input | SCLK_OUT | Input |
| | | | | | SCLK_OE | Input |
| SPI_MOSI | CDI0 | Input | Input/Output | Input/Output | MOSI_IN | Output |
| | | | | | MOSI_OUT | Input |
| | | | | | MOSI_OE | Input |
| SPI_MISO | CDI1 | Output | Input/Output | Input/Output | MISO_IN | Output |
| | | | | | MISO_OUT | Input |
| | | | | | MISO_OE | Input |
| SPI_WP | CDI2 | Input | Input | Input/Output | WP_N_IN | Output |
| | | | | | WP_N_OUT | Input |
| | | | | | WP_N_OE | Input |
| SPI_HOLD_N | CDI3 | Input | Input | Input/Output | HOLD_N_IN | Output |
| | | | | | HOLD_N_OUT | Input |
| | | | | | HOLD_N_OE | Input |

The following table shows the address mapping of the device. The entire memory area is divisible into regions of varying sizes, such as blocks (64 KB / 32 KB), sectors, and pages. These memory areas, and the relative size of memory areas, can be erased or changed with a corresponding command (see Table 6: Supporting Commands (Standard SPI) on page 16). Be aware that the page size is 256 Bytes, which corresponds with the maximum byte size that can be programmed to the flash using a single page program command.

*Table 2: Address Mapping*

| 32K Block | 64K Block | Sector | Page | Address Range | |
|---|---|---|---|---|---|
| | | | | Start | End |
| 0 | 0 | 0H | 0H | 000000H | 0000FFH |
| | | | 1H | 000100H | 0001FFH |
| | | | - | - | - |
| | | | EH | 000E00H | 000EFFH |
| | | | FH | 000F00H | 000FFFH |
| | | - | - | - | - |
| | | 7H | 70H | 007000H | 0070FFH |
| | | | 71H | 007100H | 0071FFH |
| | | | - | - | - |
| | | | 7EH | 007E00H | 007EFFH |
| | | | 7FH | 007F00H | 007FFFH |
| | 1 | 8H | 80H | 008000H | 0080FFH |
| | | | 81H | 008100H | 0081FFH |
| | | | - | - | - |
| | | | 8EH | 008E00H | 008EFFH |
| | | | 8FH | 008F00H | 008FFFH |
| | | - | - | - | - |
| | | FH | F0H | 00F000H | 00F0FFH |
| | | | F1H | 00F100H | 00F1FFH |
| | | | - | - | - |
| | | | FEH | 00FE00H | 00FEFFH |
| | | | FFH | 00FF00H | 00FFFFH |
| 1 | 2 | 10H – 17H | 100H – 17FH | 010000H | 017FFFH |
| | 3 | 18H – 1FH | 180H – 1FFH | 018000H | 01FFFFH |
| 2 | 4 – 5 | 20H – 2FH | 200H – 2FFH | 020000H | 02FFFFH |
| 3 | 6 – 7 | 30H – 3FH | 300H – 3FFH | 030000H | 03FFFFH |
| - | - | - | - | - | - |
| 28 | 56 – 57 | 1C0H – 1CFH | 1C00H – 1CFFH | 1C0000H | 1CFFFFH |
| 29 | 58 – 59 | 1D0H – 1DFH | 1D00H – 1DFFH | 1D0000H | 1DFFFFH |
| 30 | 60 | 1E0H – 1E7H | 1E00H – 1E7FH | 1E0000H | 1E7FFFH |
| | 61 | 1E8H – 1EFH | 1E80H – 1EFFH | 1E8000H | 1EFFFFH |
| 31 | 62 | 1F0H | 1F00H | 1F0000H | 1F00FFH |
| | | | 1F01H | 1F0100H | 1F01FFH |
| | | | - | - | - |
| | | | 1F0EH | 1F0E00H | 1F0EFFH |
| | | | 1F0FH | 1F0F00H | 1F0FFFH |

| 32K Block | 64K Block | Sector | Page | Address Range | |
|---|---|---|---|---|---|
| | | | | Start | End |
| 31 | 62 | - | - | - | - |
| | | 1F7H | 1F70H | 1F7000H | 1F70FFH |
| | | | 1F71H | 1F7100H | 1F71FFH |
| | | | - | - | - |
| | | | 1F7EH | 1F7E00H | 1F7EFFH |
| | | | 1F7FH | 1F7F00H | 1F7FFFH |
| | 63 | 1F8H | 1F80H | 1F8000H | 1F80FFH |
| | | | 1F81H | 1F8100H | 1F81FFH |
| | | | - | - | - |
| | | | 1F8EH | 1F8E00H | 1F8EFFH |
| | | | 1F8FH | 1F8F00H | 1F8FFFH |
| | | - | - | - | - |
| | | 1FFH | 1FF0H | 1FF000H | 1FF0FFH |
| | | | 1FF1H | 1FF100H | 1FF1FFH |
| | | | - | - | - |
| | | | 1FFEH | 1FFE00H | 1FFEFFH |
| | | | 1FFFH | 1FFF00H | 1FFFFFH |

The following table shows the Status Register bits supported by the device.

*Table 3: Status Registers*

| Bit | Name | Description | Non-Volatile | Write | Read |
|---|---|---|---|---|---|
| 0[1] | WIP | 1: Indicating whether the memory is busy in program/erase/write status register progress. | | ✓ | |
| 1[1] | WEL | 1: Enable to accept write commands (Write Status Register, Program, or Erase command). | | ✓ | ✓ |
| 6[1] – 2[1] | BP[4:0] | The Block Protect bits define the size of the area to be software protected against Program and Erase commands | ✓ | ✓ | ✓ |
| 8[2] – 7[1] | SRP[1:0] | The SRP bits control the method of write protection | ✓ | ✓ | ✓ |
| | | 00: Status register S23 – S0 can be written to after a Write Enable command (0x06), | | | |
| | | 01: Hardware Protected:<br>WP_N=0: Status registers are locked and cannot be written to.<br>WP_N=1: Status registers are unlocked and can be written to after a Write Enable command (0x06).<br>**Note:** If QE bit is set to 1, WP# pin will not function. | | | |

[1] Read Status Register with Command 0x05
[2] Read Status Register with Command 0x35

| Bit | Name | Description | Non-Volatile | Write | Read |
|---|---|---|---|---|---|
| | | 10: Command, WEL=1.<br>Power Supply Lock-Down: Status Registers are protected and cannot be written to again until the next Power up cycle. | | | |
| | | 11: Not supported | | | |
| 9[2] | QE | The Quad Enable (QE) bit allows quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enabled.<br>When the QE pin is set to 1, the quad IO2 and IO3 pins are enabled. | ✓ | ✓ | ✓ |
| 10[2] | – | Not available | | | ✓ |
| 13[2] – 11[2] | LB[3:1] | The LB3–LB1bits are one-time programmable. When set to 1, the Security Registers are permanently set to read-only. | OTP | ✓ | ✓ |
| 14[2] | CMP | Used in conjunction with bits BP4-BP0 to provide greater flexibility for array protection. | ✓ | ✓ | ✓ |
| 15[2] | SUS | 1: After executing an Program/Erase Suspend (75H) command.<br>0: By Program/Erase Resume (7AH) command, as well as a power-down, power-up cycle. | | | ✓ |
| 16[3] | – | Not available (Set to 0) | | | ✓ |
| 17[3] | – | Not available (Set to 0) | | | ✓ |
| 18[3] | WPS | 0 (default): The device uses the combination of CMP and BP[4:0] bits to protect a specific area of the memory array.<br>1: The device uses the individual block locks to protect any individual sector or blocks. | ✓ | ✓ | ✓ |
| 19[3] | – | Not available (Set to 0) | | | ✓ |
| 20[3] | – | Not available (Set to 0) | | | ✓ |
| 21[3] | – | Not available (Set to 0) | | | ✓ |
| 22[3] | – | Not available (Set to 0) | | | ✓ |
| 23[3] | HOLD/ RST | 0: The pin acts as /HOLD<br>1: The pin acts as /RESET.<br>QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin. | ✓ | ✓ | ✓ |

**Note:** Status registers S7–S0 are accessed by command 05h and 01h. Status registers S15–S8 are accessed by command 35h and 31h. Status registers S23–S16 are accessed by command 15h and 11h.

[3] Read Configure Register with Command 0x15

# SPI Flash Block Interface Support Devices

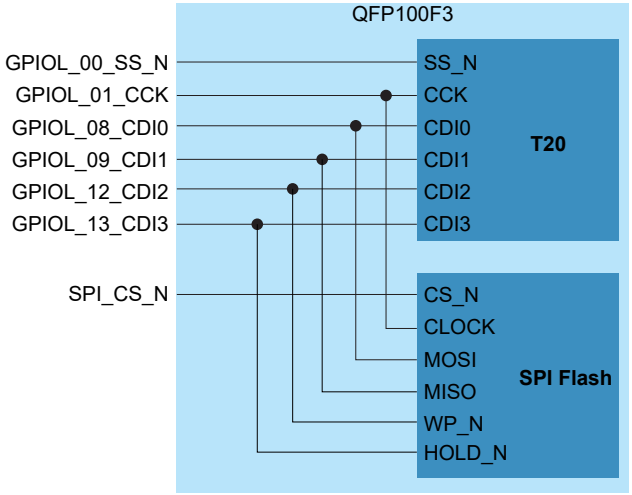
This section describes the SPI flash interface for Efinix system-in-package (SIP) FPGAs that include an internal SPI flash device.

## Trion Devices

Trion FPGAs in QFP100F3 packages are a system-in-package (SIP) that includes an internal SPI flash device.

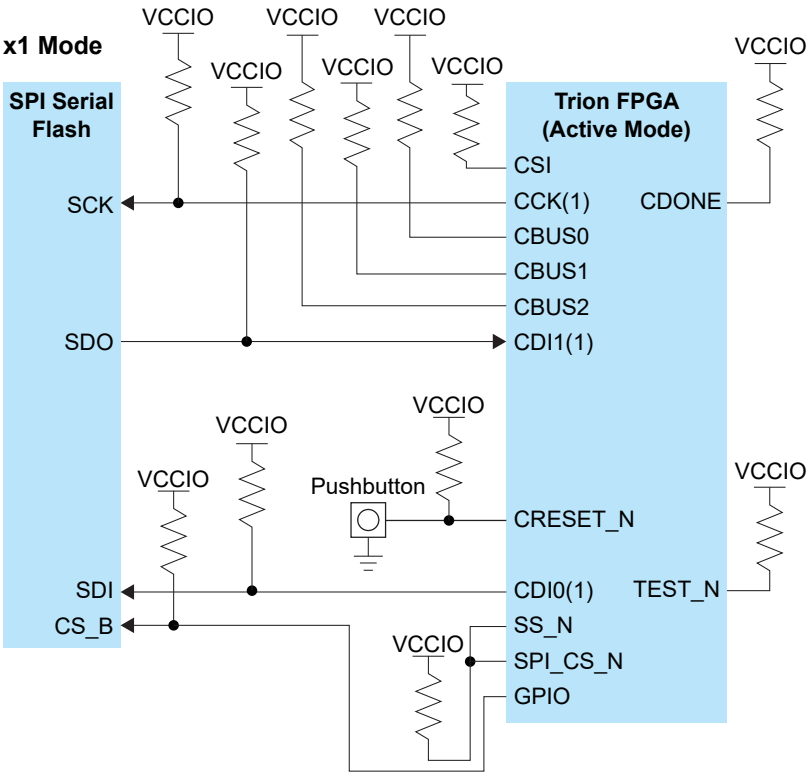
The SPI flash memory VCC is powered by `VCCIO1A_1B_1C` (3.3 V)[4]. The following figure shows the internal connections and pin assignment. The SPI flash memory stores the configuration bitstream for FPGA SPI active configurations. The SPI flash device is used to store the bitstream. Additionally, in user mode, the SPI flash device can store data sent to it by the FPGA. For a more detailed overview of FPGA hardware design and configuration, refer to **AN 006: Configuring Trion FPGAs**. The CS pin of the internal SPI flash device is an individual pin in the package. Connect the pin to `GPIOL_00_SS_N` on the board design if you intend to use the internal flash.

*Figure 1: Connections between FPGA and SPI Flash Device inside the Package*



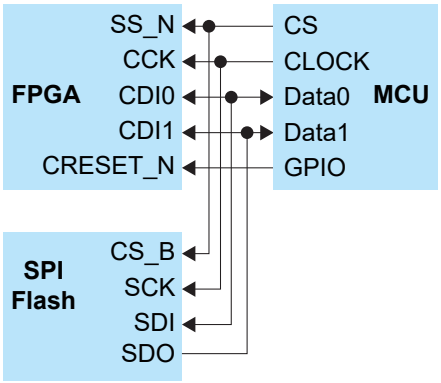

[4] The I/O bank and flash on the Trion T20 can operate on 1.8 V.

*Figure 2: Circuit Design using both Internal and External Flash*




Note:
1. External pull-up is optional unless required by an external load.

*Figure 3: Shared SPI Bus Connections*

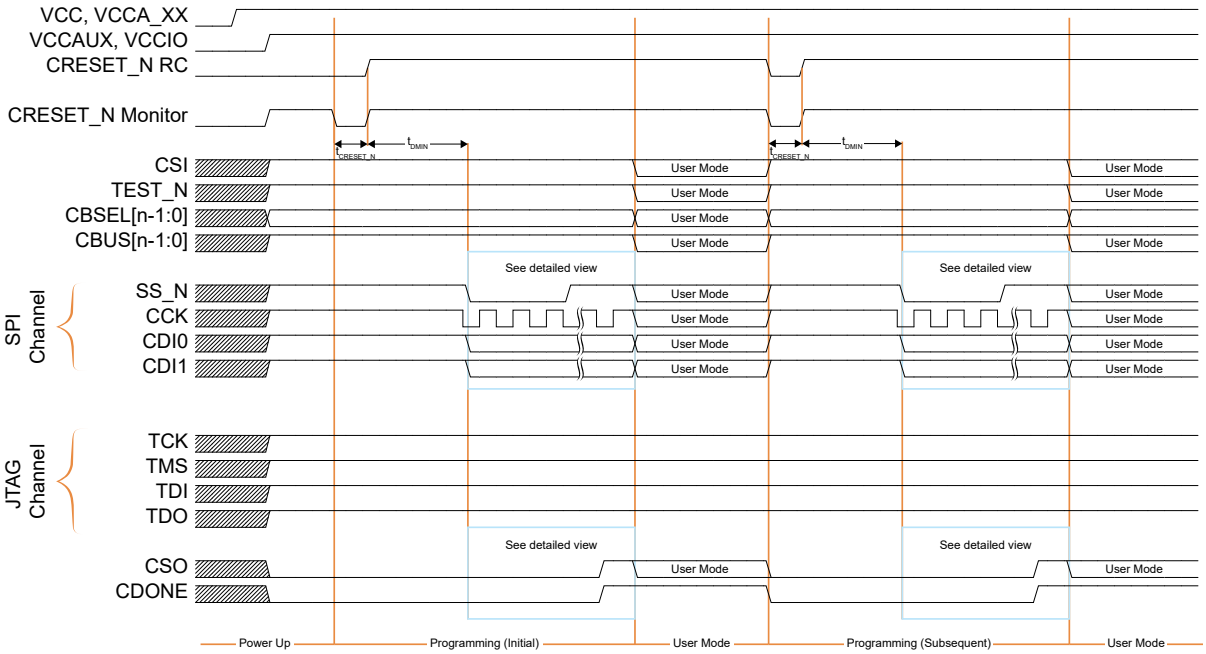



**Note:** To program the SPI flash or to enter SPI passive configuration, the off-chip MCU should:

- Drive `SS_N` to low
- Drive `CRESET_N` to low.

If the FPGA is configurated in SPI Active mode, please consider the correct timing sequence before accessing the SPI interface in user mode.

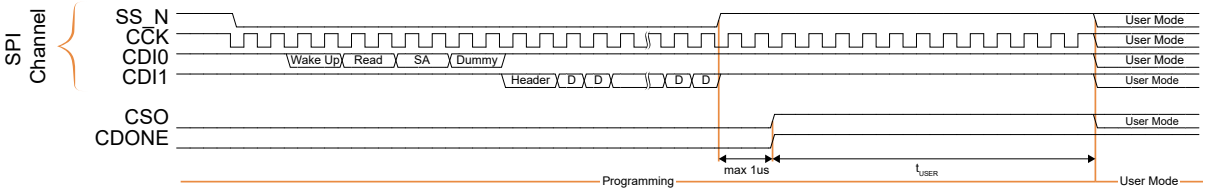
*Figure 4: SPI Active (x1) Configuration*




**Note:**

CRESET_N RC refers to the CRESET_N pin connected to an RC circuit that delays the voltage supplied to the pin after power-up.
CRESET Monitor refers to the CRESET_N pin connected to a pull-up resistor, where the supplied voltage is the same as VCCIO.

*Figure 5: SPI Active (x1) Configuration (Detailed View)*




**Legend:**

SA: Start Address D: Data

For advice on enabling the SPI flash device in your design, refer to Chapter 11 SPI Flash Interface in the Trion Interfaces User Guide.

## Titanium Devices

Titanium FPGAs in F100F3S2 packages are a system-in-package (SIP) that includes an internal SPI flash device.

The SPI flash memory VCC is connected to `VCCIO1A_4B`. If you are using the SPI flash memory, drive the `VCCIO1A_4B` with a 1.8 V supply. The following figure shows the internal connections and pin assignment. The SPI flash memory stores the configuration bitstream for FPGA SPI active configurations. The SPI flash device is used to store the bitstream. Additionally, in user mode, the SPI flash device can store data sent to it by the FPGA. For a more detailed overview of FPGA hardware design and configuration, refer to **AN 033: Configuring Titanium FPGAs**.

*Figure 6: Connections between FPGA and SPI Flash inside the Package*

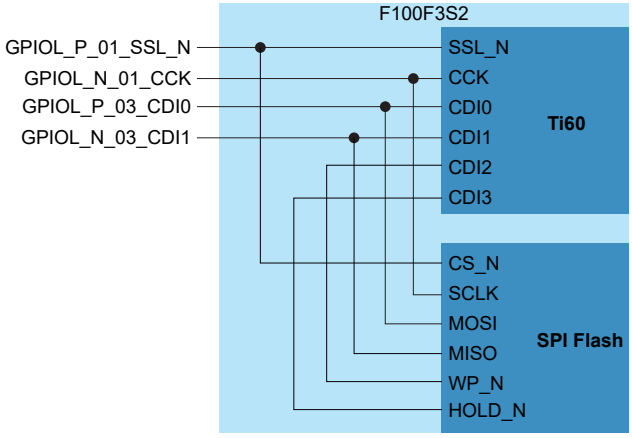
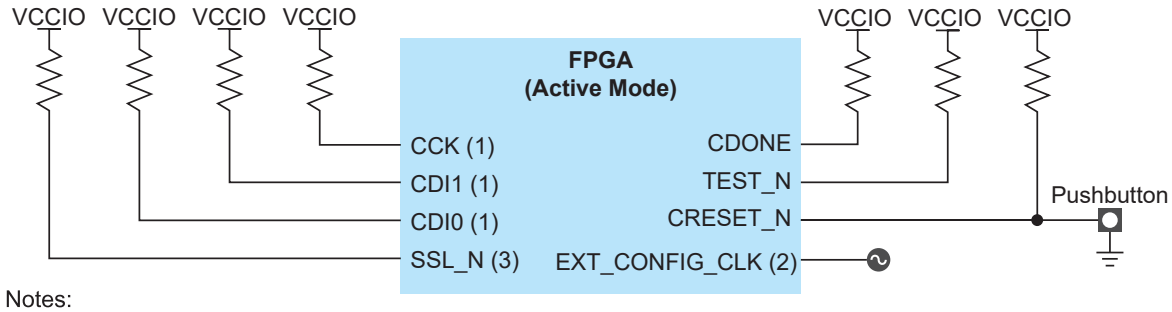


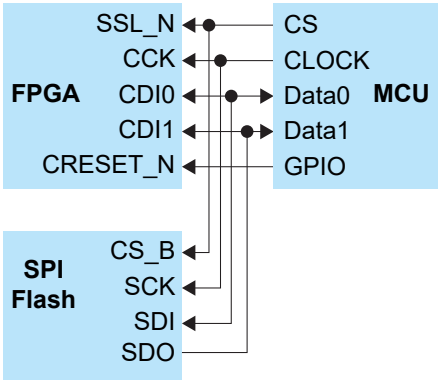

*Figure 7: Configuration with Internal Flash*




Notes:

1. The external pull-up is optional unless required by an external load.
2. Connect the EXT_CONFIG_CLK to an external clock source if the clock source is selected as an external clock in the Efinity **Project Editor > Bitstream Generation** tab.
3. Only use the SSL_N pin as the GPIO to access the internal flash.

*Figure 8: Shared SPI Bus Connections*

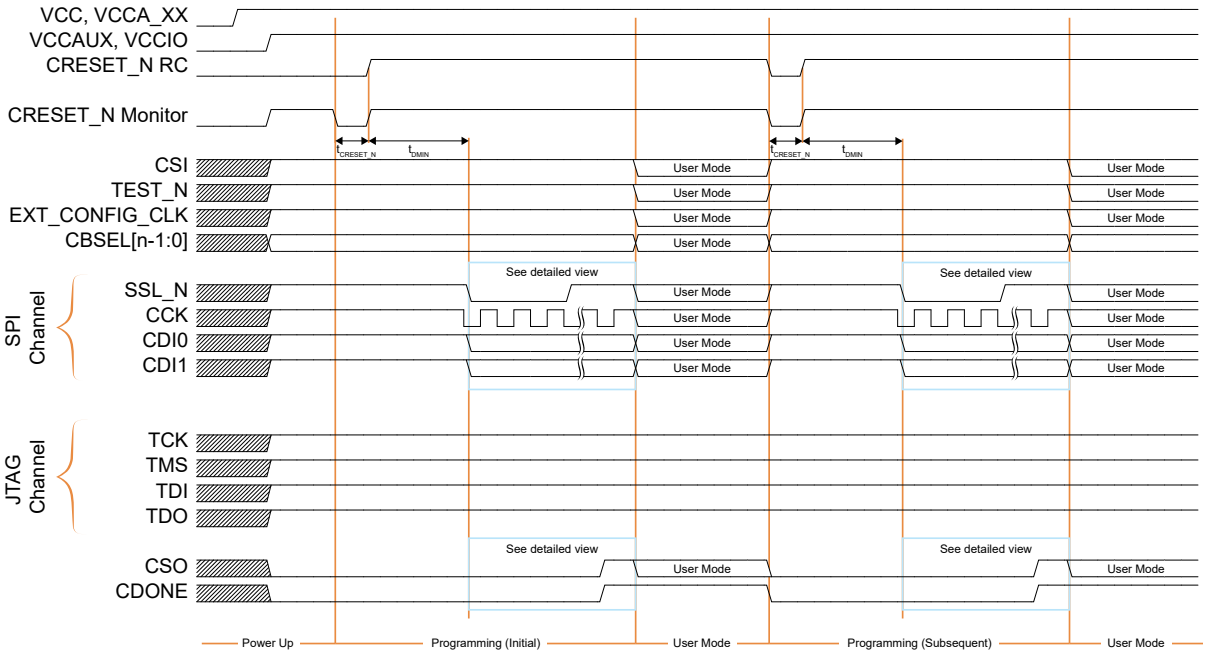



**Note:** To program the SPI flash or to enter SPI passive configuration, the off-chip MCU should:

- Drive `SSL_N` to low
- Drive `CRESET_N` to low.

If the FPGA is configurated in SPI Active mode, please consider the correct timing sequence before accessing the SPI interface in user mode.

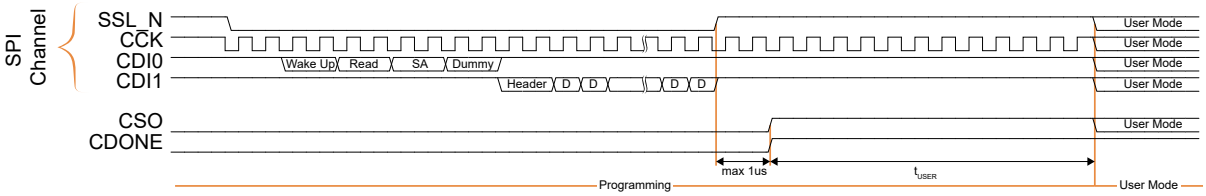
*Figure 9: SPI Active (x1) Configuration*




**Note:**

CRESET_N RC refers to the CRESET_N pin connected to an RC circuit that delays the voltage supplied to the pin after power-up.
CRESET Monitor refers to the CRESET_N pin connected to a pull-up resistor, where the supplied voltage is the same as VCCIO.

*Figure 10: SPI Active (x1) Configuration (Detailed View)*




**Legend:**

SA: Start Address D: Data

For enabling the SPI flash block in Design , please reference to Chapter 14 SPI Flash Interface of Titanium Interfaces User Guide.

# Timing and AC Characteristics

The following figures show the timing of serial input/output data transmitted between the FPGA interface (master) and SPI flash device, as well as corresponding AC characteristics.

*Figure 11: Serial Output Timing*

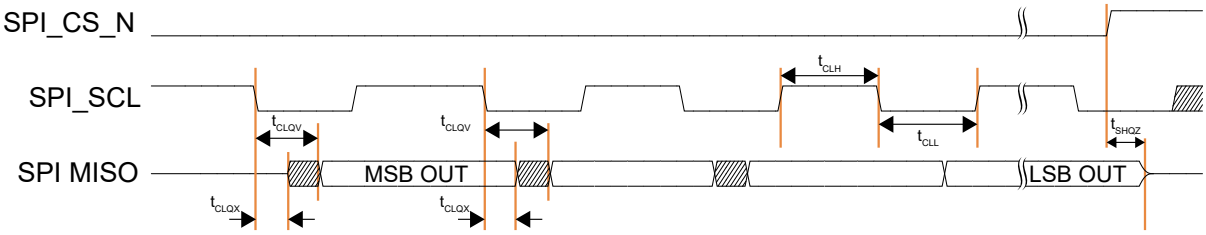



*Figure 12: Serial Input Timing*

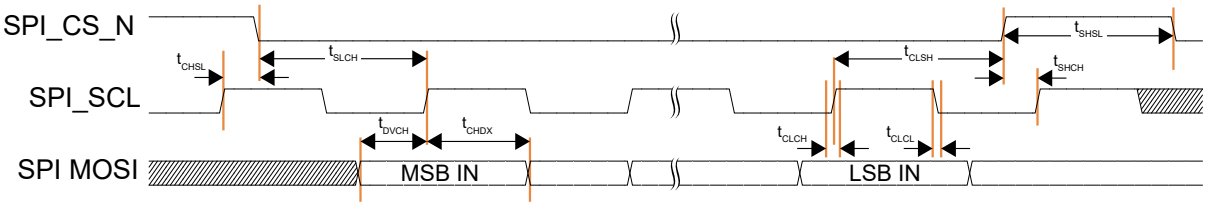



*Table 4: AC Parameters for Interfacing with SPI Flash ($T_a$ = -40°C to +85°C)*

| Symbol | Parameter | VCC = 1.8 V[5] | | | VCC = 3.3 V[6] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $f_{SCLK}$ | Clock Frequency | | | 33 | | | 55 | MHz |
| $t_{CLL}$ | Clock High Time | 5.5 | | | 3.3 | | | ns |
| $t_{CLH}$ | Clock Low Time ($f_{SCLK}$) 45% x (1$f_{SCLK}$) | 5.5 | | | 3.3 | | | ns |
| $t_{CLQX}$ | Output Hold Time | 0 | | | 0 | | | ns |
| $t_{CLQV}$ | Clock Low to Output Valid Loading | 7 | | | 7 | | | ns |
| $t_{SHQZ}$ | Output Disable Time | | | 6 | | | 6 | ns |
| $t_{CHSL}$ | CS# Not Active Hold Time (Relative to SCLK) | 5 | | | 5 | | | ns |
| $t_{SLCH}$ | CS# Active Setup Time (Relative to SCLK) | 5 | | | 5 | | | ns |
| $t_{DVCH}$ | Data in Setup Time | 2 | | | 2 | | | ns |
| $t_{CHDX}$ | Data in Hold Time | 3 | | | 3 | | | ns |
| $t_{CLCH}$ | Clock Rise Time (Peak to Peak) | 0.1 | | | 0.1 | | | V/ns |
| $t_{CHCL}$ | Clock Fall Time (Peak to Peak) | 0.1 | | | 0.1 | | | V/ns |
| $t_{SHSL}$ | CS# Deselect Time from Read to next Read | 20 | | | 20 | | | ns |
| $t_{SHSL}$ | CS# Deselect Time From Write, Erase, Program to Read Status Register | 30 | | | 30 | | | ns |
| $t_{CHHL}$ | HOLD# Not Active Hold Time (Relative to SCLK) | 5 | | | 5 | | | ns |

(5) All Titanium products run SPI flash at 1.8 V.
(6) All Trion products run SPI flash at 3.3 V. The Trion T20 can run SPI flash at either 1.8 V or 3.3 V.

| Symbol | Parameter | VCC = 1.8 V[5] | | | VCC = 3.3 V[6] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $t_{HLCH}$ | HOLD# Active Setup Time (Relative to SCLK) | 5 | | | 5 | | | ns |
| $t_{CHHH}$ | HOLD# Active Hold Time (Relative to SCLK) | 5 | | | 5 | | | ns |
| $t_{HHCH}$ | HOLD# Not Active Setup Time (Relative to SCLK) | 5 | | | 5 | | | ns |
| $t_{HLQZ}$ | HOLD# to Output High-Z | | | 6 | | | 6 | ns |
| $t_{HHQX}$ | Output Hold Time | | | 6 | | | 6 | ns |
| $t_{WHSL}$ | Write Protect Setup Time | 20 | | | 20 | | | ns |
| $t_{SHWL}$ | Write Protect Hold Time | 100 | | | 100 | | | ns |
| $t_{DP}$ | CS# High to Deep Power-down Mode | | | 3 | | | 3 | us |
| $t_{RES1}$ | CS# High to Standby Mode without Electronic Signature Read | | | 8 | | | 8 | us |
| $t_{RES2}$ | CS# High to Standby Mode with Electronic Signature Read | | | 8 | | | 8 | us |
| $t_W$ | Write Status Register Cycle Time | | 8 | 12 | | 8 | 12 | ms |
| $t_{Ready}$ | Reset Recovery Time (for erase/program operation except WRSR) | 30 | | | 30 | | | us |
| | Reset Recovery Time (for WRSR operation) | 12 | 8 | | 12 | 8 | | ms |
| $t_{BL}$ | Load memory page data to buffer time (256 Byte) | | | 60 | | | 60 | us |
| | Load memory page data to buffer time (512 Byte) | | | 120 | | | 120 | us |
| $t_{BC}$ | Buffer clear to next instruction latency | 300 | | | 200 | | | ns |

(5) All Titanium products run SPI flash at 1.8 V.
(6) All Trion products run SPI flash at 3.3 V. The Trion T20 can run SPI flash at either 1.8 V or 3.3 V.

The following waveforms show the timing of hold and WP between the FPGA interface (master) and SPI flash device, as well as corresponding AC characteristics as shown previously.

*Figure 13: Hold Timing*

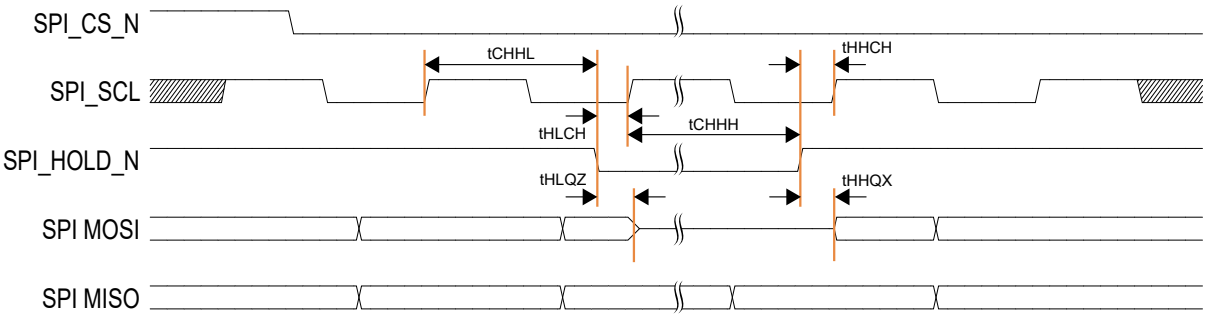
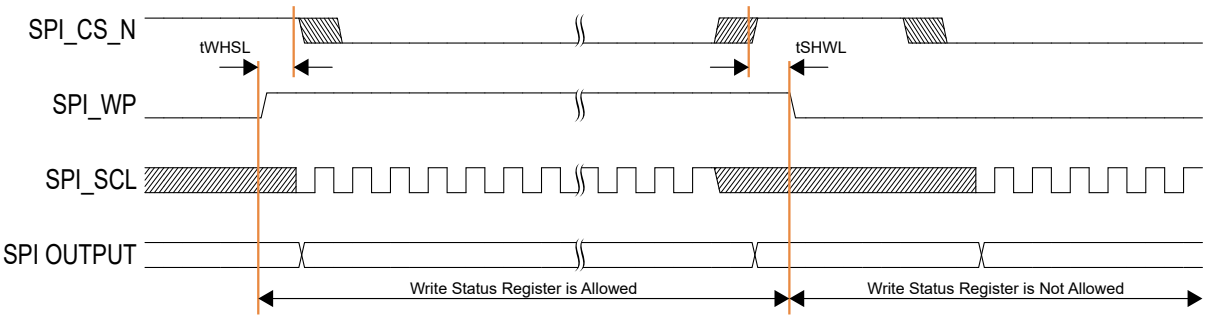



*Figure 14: WP Timing*




The following table shows the timing of Program and Erase command operations.

*Table 5: AC Parameters for SPI Flash Program and Erase ($T_a$ = -40°C to +85°C)*

| Symbol | Parameter | VCC = 1.8 V[7] | | | VCC = 3.3 V[8] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| TESL | Erase Suspend Latency | | | 30 | | | 30 | us |
| TPSL | Program Suspend Latency | | | 30 | | | 30 | us |
| TPRS | Latency between Program Resume and Next Suspend | 20 | | | 20 | | | us |
| TERS | Latency between Erase Resume and next Suspend | 20 | | | 20 | | | us |
| $t_{PP}$ | Page program time (up to 256 bytes) | | 2 | 3 | | 1.5 | 3 | ms |
| $t_{PE}$ | Page erase time | | 16 | 20 | | 16 | 30 | ms |
| $t_{SE}$ | Sector erase time | | 16 | 20 | | 16 | 30 | ms |
| $t_{BE1}$ | Block erase time for 32K bytes | | 16 | 20 | | 16 | 30 | ms |
| $t_{BE2}$ | Block erase time for 64K bytes | | 16 | 20 | | 16 | 30 | ms |
| $t_{CE}$ | Chip erase time | | 130 | 180 | | 130 | 180 | ms |

[7] All Titanium products run SPI flash at 1.8 V.
[8] All Trion products run SPI flash at 3.3 V. The Trion T20 can run SPI flash at either 1.8 V or 3.3 V.

# Supporting Commands

The following table shows a list of commands used to support SPI flash memory blocks. Memory access supports 24-bit addressing, with byte addresses assigned via the address frame. The first byte on the frame is at the address [23:16], followed by address [15:8], and with the last byte at address [7:0]. All serial input and output timing frames for standard SPI commands rely on x1 mode timing.

For dual SPI commands, some serial input/output timings rely on x2 mode timing. Pins `SPI_MOSI` and `SPI_MISO` are used for either serial input or output. `SPI_WP` and `SPI_HOLD` pin functions are available.

For quad SPI commands, some serial input /output timings rely on x4 mode timing. `SPI_MOSI`, `SPI_MISO`, `SPI_WP` and `SPI_HOLD` are used for either serial input or output. The QE bit of the status registers must be set to 1 before issuing any quad SPI commands. Also, be aware the functions of the `SPI_WP` and `SPI_HOLD` pins are unavailable while the QE bit is set to 1.

*Table 6: Supporting Commands (Standard SPI)*

| Commands | Description | Value / Number of Bytes (Mode) | | | | |
|---|---|---|---|---|---|---|
| | | Op Code (Command) | Address | Dummy | Data Input | Data Output |
| **Status Register** | | | | | | |
| Read Status Register | Read Status Register Bit S7 – S0 (see Fig. 16) | 05h (x1) | | | S7 – S0 (x1) | |
| Read Status Register-1 | Read Status Register Bit S15 – S8 (see Fig. 16) | 35h (x1) | | | S15 – S8 (x1) | |
| Read Configure Register-2 | Read Status Register Bit S23 – S16 (see Fig. 16) | 15h (x1) | | | S23 – S16 (x1) | |
| Write Status Register | Write to Status Register Bits S7 – S0 (see Fig. 15) | 01h (x1) | | | | S7 – S0 (x1) |
| Write Status Register-1 | Write to Status Register Bits S15 – S8 (see Fig. 15) | 31h (x1) | | | | S15 – S8 (x1) |
| Write Configure Register-2 | Write to Status Register Bits S23 – S16 (see Fig. 15) | 11h (x1) | | | | S23 – S16 (x1) |
| **Read** | | | | | | |
| Read Array | *n* Bytes Read Until CS# Goes High (see Fig. 16) | 03h (x1) | 3 (x1) | | 1+ (x1) | |
| Read Array (Fast) | *n* Bytes Read Until CS# Goes High (see Fig. 16) | 0Bh (x1) | 3 (x1) | 1 (x1) | 1+ (x1) | |

| Commands | Description | Value / Number of Bytes (Mode) | | | | |
|---|---|---|---|---|---|---|
| | | Op Code (Command) | Address | Dummy | Data Input | Data Output |
| Read Manufacturer/ Device ID | Output JEDEC ID: 1-Byte Manufacturer ID 2-Byte Device ID (see Fig. 16) | 9Fh (x1) | | | 1 – 3 (x1) | |
| Read Manufacture ID | Read Manufacturer ID (Odd Address) and Device ID (Even Address) (see Fig. 16) | 90h (x1) | 3 (x1) | | 1+ (x1) | |
| **Erase/Program** | | | | | | |
| Page Erase | Erase Selected Page (see Fig. 15) | 81h (x1) | 3 (x1) | | | |
| Sector Erase (4K Bytes) | Erase Selected Sector (see Fig. 15) | 20h (x1) | 3 (x1) | | | |
| Block Erase (32K Bytes) | Erase Selected 32K Block (see Fig. 15) | 52h (x1) | 3 (x1) | | | |
| Block Erase (64K Bytes) | Erase Selected 64K Block (see Fig. 15) | D8h (x1) | 3 (x1) | | | |
| Chip Erase | Erase Whole Chip (see Fig. 15) | 60h/C7h (x1) | | | | |
| Page Program | Program Selected Page (see Fig. 15) | 02h (x1) | 3 (x1) | | | 1 – 256 (x1) |
| Program/Erase Suspend | Suspend Program/ erase Operation (see Fig. 15) | 75h (x1) | | | | |
| Program/Erase Resume | Suspend Program/ Erase Operation (see Fig. 15) | 7Ah (x1) | | | | |
| **Protection** | | | | | | |
| Write Enable | Sets Write Enable Latch Bit S1 WEL = 1 (see Fig. 15) | 06h (x1) | | | | |
| Write Disable | Resets Write Enable Latch Bit S1 WEL = 0 (see Fig. 15) | 04h (x1) | | | | |
| Volatile SR Write Enable | Write Enable for Volatile SR (see Fig. 15) | 50h (x1) | | | | |
| Individual Block Lock | Individual Block Lock (see Fig. 15) | 36h (x1) | 3 (x1) | | | |
| Individual Block Unlock | Individual Block Lock (see Fig. 15) | 39h (x1) | 3 (x1) | | | |
| Read Block Lock Status | Read Individual Block Lock Register (see Fig. 16) | 3Dh (x1) | 3 (x1) | | 1+ (x1) | |

| Commands | Description | Value / Number of Bytes (Mode) | | | | |
|---|---|---|---|---|---|---|
| | | Op Code (Command) | Address | Dummy | Data Input | Data Output |
| Global Block Lock | Whole Chip Block Protect (see Fig. 15) | 7Eh (x1) | | | | |
| Global Block Unlock | Whole Chip Block Unprotect (see Fig. 15) | 98h (x1) | | | | |
| **Security** | | | | | | |
| Erase Security Registers | Erase Security Registers (see Fig. 15) | 44h (x1) | 3 (x1) | | | |
| Program Security Registers | Program Security Registers (see Fig. 15) | 42h (x1) | 3 (x1) | | | 1+ (x1) |
| Read Security Registers | Read Value of Security Registers (see Fig. 16) | 48h (x1) | 3 (x1) | | 1+ (x1) | |
| **Others (Standard SPI)** | | | | | | |
| Reset Enable | Enable Reset (see Fig. 15) | 66h (x1) | | | | |
| Reset | Enable Reset (see Fig. 15) | 99h (x1) | | | | |
| Deep Power Down | Enters Deep Power-Down Mode (see Fig. 15) | B9h (x1) | | | | |
| Release Deep Power - Down/ Read Electronic ID | Read Eelectronic ID Data (see Fig. 16) | Abh (x1) | 3 (x1) | | 1 (x1) | |
| Read SFDP | Read SFDP Parameter (SFDP is a JEDEC Standard, JESD216B) (see Fig. 16) | 5Ah (x1) | 3 (x1) | 1 (x1) | 1+ (x1) | |

*Table 7: Supporting Commands (Dual and Quad SPI)*

| Commands | Description | Value / Number of Bytes (Mode) | | | | |
|---|---|---|---|---|---|---|
| | | Op Code (Command) | Address | Dummy | Data Input | Data Output |
| **Read (Dual SPI)** | | | | | | |
| Read Dual Output | *n* Bytes Read by Dual Output (see Fig. 17) | 3Bh (x1) | 3 (x1) | 1 (x1) | 1+ (x2) | |
| Read 2IO | *n* Bytes Read by 2IO (see Fig. 17) | BBh (x1) | 3 (x2) | 1 (x1) | 1+ (x1) | |
| Dual Read Manufacture ID | Dual Output Manufacture (Odd)/Device ID (Even) (see Fig. 17) | 92h (x1) | 3 (x2) | | 1+ (x2) | |
| **Read (QUAD SPI)** | | | | | | |
| Read QUAD Output | *n* bytes read out by quad output (see Fig. 18) | 6Bh (x1) | 3 (x1) | 1 (x1) | 1+ (x4) | |
| Read 4IO | *n* Bytes Read by 4IO (see Fig. 18) | Ebh (x1) | 3 (x4) | 3 (x4) | 1+ (x4) | |
| Read Word 4IO | *n* Bytes Word Read by 4IO (see Fig. 18) | E7h (x1) | 3 (x4) | 1 (x4) | 1+ (x4) | |
| Quad Read Manufacture ID | Quad Output Manufacture (Odd)/Device ID (Even Address) (see Fig. 18) | 94h (x1) | 3 (x4) | | 1+ (x4) | |
| **Erase / Program (QUAD SPI)** | | | | | | |
| Quad Page Program | Quad Input to Program Selected Page (see Fig. 19) | 32h (x1) | 3 (x1) | | | 1 – 256 (x4) |

*Figure 15: Timing for Standard SPI Command and Optional Write Data to SPI Flash in Standard SPI Mode*

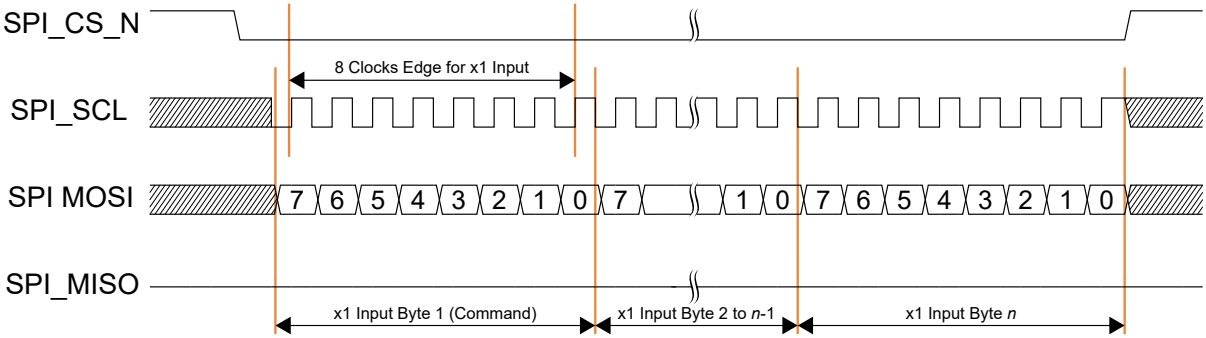



*Figure 16: Timing for Standard SPI Command and Optional Data Read from SPI Flash in Standard SPI Mode*

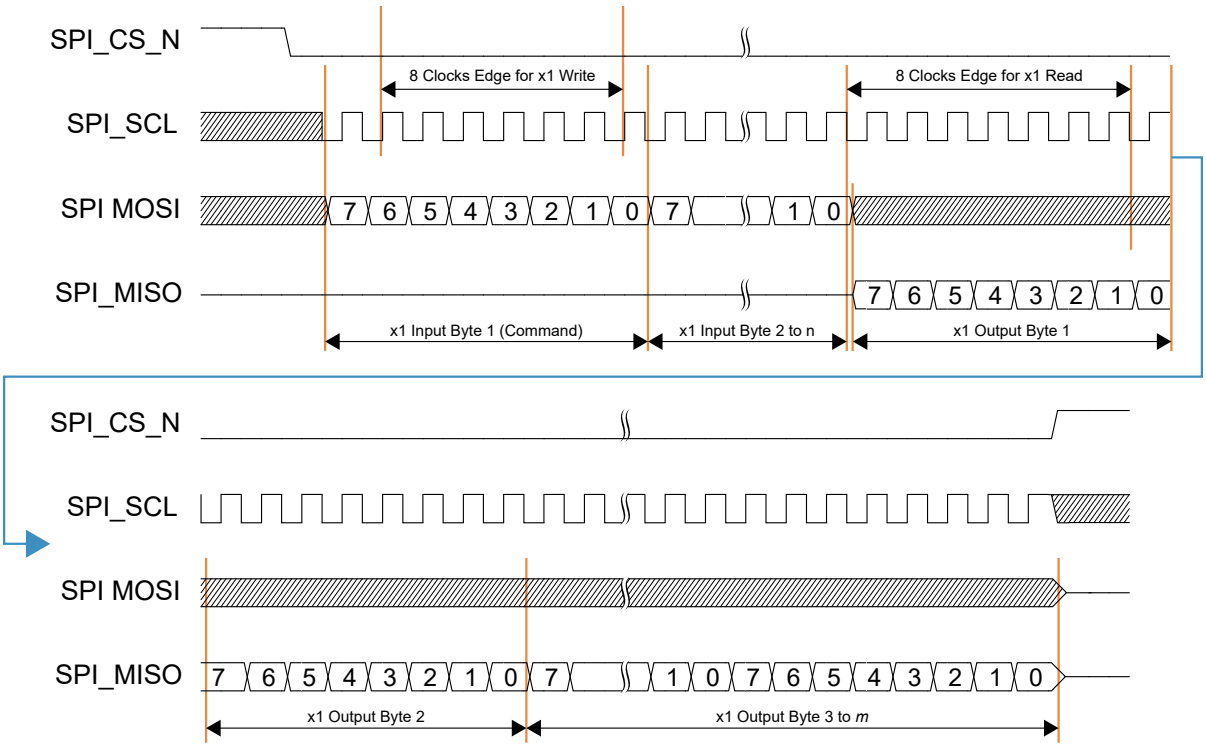


*Figure 17: Timing for Standard SPI Command and Optional Data Read from SPI Flash in Dual-SPI Mode*

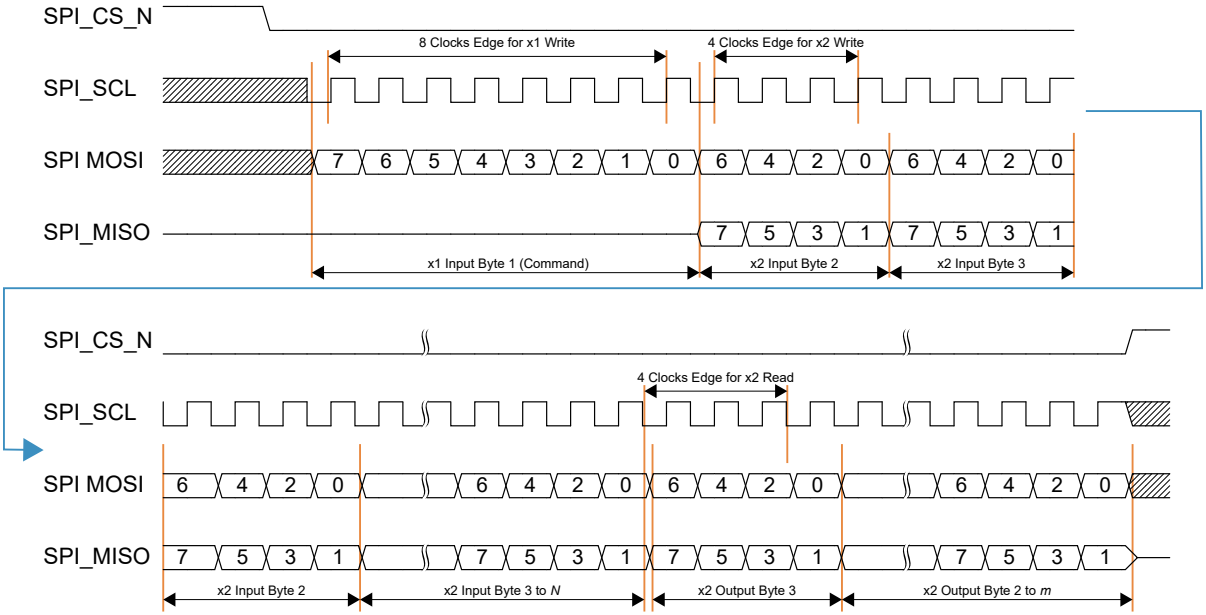



*Figure 18: Timing for Standard SPI Command and Optional Data Read from SPI Flash in Quad Mode*

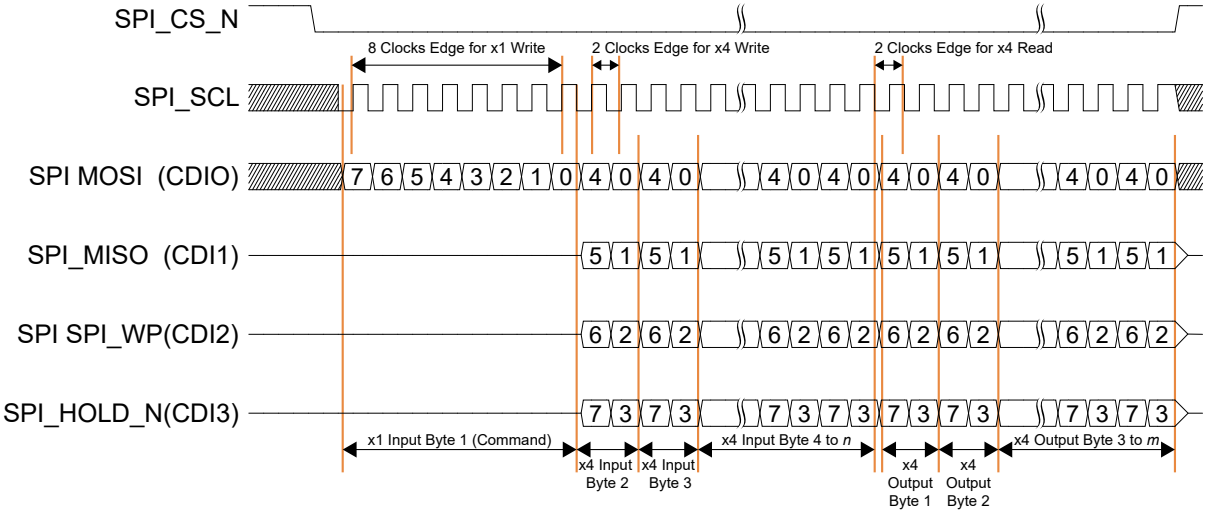
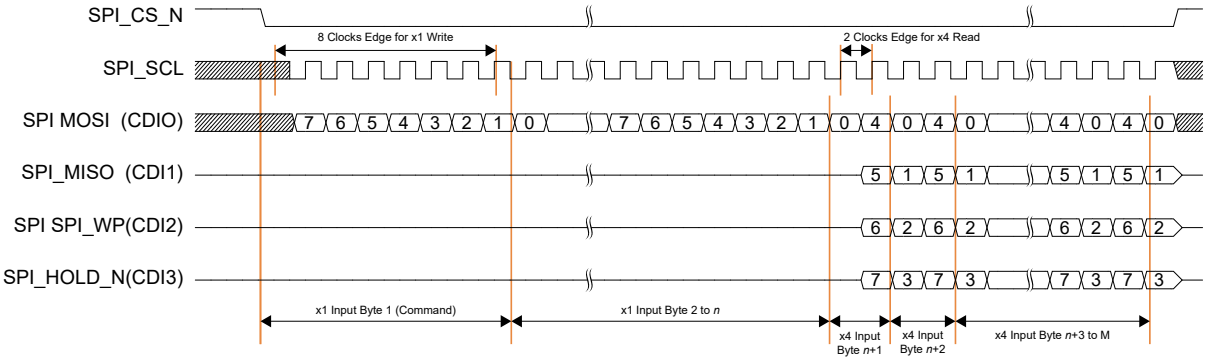



*Figure 19: Timing for Standard SPI Command and Optional Data Write from SPI Flash in Quad Mode*



# Data Protection

The BP[4:0] and CMP WPS status registers are used to define protected areas of memory. Any commands, whether issued manually by automated by software, to change or erase the content of these protected memory blocks is ignored. These protected memory blocks are listed in the following tables.

*Table 8: Write Protection Area IF WPS = 0 and CMP Bit = 0*

Protected Area Sizes (WPS = 0, CMP Bit = 0)

| Status Bit | | | | | Memory Content | | | | Portion |
|---|---|---|---|---|---|---|---|---|---|
| BP4 | BP3 | BP2 | BP1 | BP0 | Blocks | Addresses | | Density | |
| | | | | | | Start | End | | |
| x | x | 0 | 0 | 0 | - | - | - | - | - |
| 0 | 0 | 0 | 0 | 1 | 31 | 1F0000 | 1FFFFF | 64 KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 0 | 30 - 31 | 1E0000 | 1FFFFF | 128 KB | Upper 1/16 |
| 0 | 0 | 0 | 1 | 1 | 28 - 31 | 1C0000 | 1FFFFF | 256 KB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 0 | 24 - 31 | 180000 | 1FFFFF | 512 KB | Upper 1/4 |
| 0 | 0 | 1 | 0 | 1 | 16 - 31 | 100000 | 1FFFFF | 1 MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 | 000000 | 00FFFF | 64 KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 0 | 0 - 1 | 000000 | 01FFFF | 128 KB | Lower 1/16 |
| 0 | 1 | 0 | 1 | 1 | 0 - 3 | 000000 | 03FFFF | 256 KB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 0 | 0 - 7 | 000000 | 07FFFF | 512 KB | Lower 1/4 |
| 0 | 1 | 1 | 0 | 1 | 0 - 15 | 000000 | 0FFFFF | 1 MB | Lower 1/2 |
| x | x | 1 | 1 | x | 0 - 31 | 000000 | 1FFFFF | 2 MB | All |
| 1 | 0 | 0 | 1 | 1 | 31 | 1FF000 | 1FFFFF | 4 KB | Upper 1/512 |
| 1 | 0 | 1 | 0 | 0 | 31 | 1FE000 | 1FFFFF | 8 KB | Upper 1/256 |
| 1 | 0 | 1 | 0 | 1 | 31 | 1FC000 | 1FFFFF | 16 KB | Upper 1/128 |
| 1 | 0 | 1 | 0 | x | 31 | 1F8000 | 1FFFFF | 32 KB | Upper 1/64 |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000 | 000FFF | 4 KB | Lower 1/512 |
| 1 | 1 | 1 | 0 | 0 | 0 | 000000 | 001FFF | 8 KB | Lower 1/256 |
| 1 | 1 | 1 | 0 | 1 | 0 | 000000 | 003FFF | 16 KB | Lower 1/128 |
| 1 | 1 | 1 | 0 | x | 0 | 000000 | 007FFF | 32 KB | Lower 1/64 |

*Table 9: Write Protection Area IF WPS = 0 and CMP Bit = 1*

Protected Area Sizes (WPS = 0, CMP Bit = 1)

| Status Bit | | | | | Memory Content | | | | Portion |
|---|---|---|---|---|---|---|---|---|---|
| BP4 | BP3 | BP2 | BP1 | BP0 | Blocks | Addresses | | Density | |
| | | | | | | Start | End | | |
| x | x | 0 | 0 | 0 | 0 – 31 | 0 | 1FFFFF | 2 MB | All |
| 0 | 0 | 0 | 0 | 1 | 0 – 30 | 000000 | 1EFFFF | 1984 KB | Lower 31/31 |
| 0 | 0 | 0 | 1 | 0 | 0 – 29 | 000000 | 1DFFFF | 1920 KB | Lower 15/16 |
| 0 | 0 | 0 | 1 | 1 | 0 – 27 | 000000 | 1BFFFF | 1792 KB | Lower 7/8 |
| 0 | 0 | 1 | 0 | 0 | 0 – 23 | 000000 | 17FFFF | 1536 KB | Lower 3/4 |
| 0 | 0 | 1 | 0 | 1 | 0 – 15 | 000000 | 0FFFFF | 1 MB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 1 – 31 | 010000 | 1FEFFF | 1984 KB | Upper 31/31 |
| 0 | 1 | 0 | 1 | 0 | 2 – 31 | 020000 | 1FEFFF | 1920 KB | Upper 15/16 |
| 0 | 1 | 0 | 1 | 1 | 4 – 31 | 0400000 | 1FEFFF | 1792 KB | Upper 7/8 |
| 0 | 1 | 1 | 0 | 0 | 8 – 31 | 080000 | 1FEFFF | 1536 KB | Upper 3/4 |
| 0 | 1 | 1 | 0 | 1 | 16 – 31 | 100000 | 1FEFFF | 1 MB | Upper 1/2 |
| x | x | 1 | 1 | x | – | – | – | – | – |
| 1 | 0 | 0 | 0 | 1 | 0 – 31 | 000000 | 1FEFFF | 2044 KB | Lower 511/512 |
| 1 | 0 | 0 | 1 | 0 | 0 – 31 | 000000 | 1FDFFF | 2040 KB | Lower 255/256 |
| 1 | 0 | 0 | 1 | 1 | 0 – 31 | 000000 | 1FBFFF | 2032 KB | Lower 127/128 |
| 1 | 0 | 1 | 0 | x | 0 – 31 | 000000 | 1F7FFF | 2016 KB | Lower 63/64 |
| 1 | 1 | 0 | 0 | 1 | 0 – 31 | 001000 | 1FFFFF | 2044 KB | Upper 511/512 |
| 1 | 1 | 0 | 1 | 0 | 0 – 31 | 002000 | 1FFFFF | 2040 KB | Upper 255/256 |
| 1 | 1 | 0 | 1 | 1 | 0 – 31 | 004000 | 1FFFFF | 2032 KB | Upper 127/128 |
| 1 | 1 | 1 | 0 | x | 0 – 31 | 008000 | 1FFFFF | 2016 KB | Upper 63/64 |

If WPS = 1, individual block/sector protection is enabled. All individual block/sector lock bits are set to 1 by default after power up, meaning that the entire memory array is protected. The following table shows the protected block/sector areas of the memory. To write to or erase the content of any of these protected block/sector areas of memor, either a command must be given to unlock an individual memory block at a specified address, or a Global Block Unlock command must be issued.

*Table 10: Individual Block Protection (WPS=1)*

| Blocks | Memory Content | | | | Block/Sector Lock Commands |
|---|---|---|---|---|---|
| | Sector | Addresses | | Density | |
| | | Start | End | | |
| 0 | 0 | 000000 | 000FFF | 4 KB | 36h, 39h, 3Dh |
| | 1 | 001000 | 001FFF | 4 KB | 36h, 39h, 3Dh |
| | - | - | - | - | - |
| | 14 | 00E000 | 00EFFF | 4 KB | 36h, 39h, 3Dh |
| | 15 | 00F000 | 00FFFF | 4 KB | 36h, 39h, 3Dh |
| 1 | All | 010000 | 01FFFF | 64 KB | 36h, 39h, 3Dh |
| 2 | All | 020000 | 02FFFF | 64 KB | 36h, 39h, 3Dh |
| 3 | All | 030000 | 03FFFF | 64 KB | 36h, 39h, 3Dh |
| - | - | - | - | - | - |
| 28 | All | 1C0000 | 1CFFFF | 64 KB | 36h, 39h, 3Dh |
| 29 | All | 1C0000 | 1CFFFF | 64 KB | 36h, 39h, 3Dh |
| 30 | All | 1E0000 | 1EFFFF | 64 KB | 36h, 39h, 3Dh |
| 31 | 496 (0) | 1F0000 | 1F0FFF | 4 KB | 36h, 39h, 3Dh |
| | 497 (1) | 1F1000 | 1F1FFF | 4 KB | 36h, 39h, 3Dh |
| | - | - | - | - | - |
| | 510 (14) | 1FE000 | 1FEFFF | 4 KB | 36h, 39h, 3Dh |
| | 511 (15) | 1FF000 | 1FFFFF | 4 KB | 36h, 39h, 3Dh |
| 0 – 31 | All | 000000 | 1FFFFF | 2 MB | 7Eh, 98h |

# Revision History

*Table 11: Revision History*

| Date | Version | Description |
|---|---|---|
| April 2025 | 1.0 | Initial release. |