



AN 067: Migrating Titanium and Topaz Designs in N484 Packages

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Introduction

Commonly, larger FPGAs are used during the development process, while smaller FPGAs are used in production. Larger FPGAs offer more logic elements, memory blocks, and DSP blocks, enabling designers to implement additional features and integrate debugging tools. However, tools such as Virtual I/O (VIO) and Logic Analyzer (LA) may not fit into the final, smaller FPGA. Once the design is finalized and optimized, it can be transferred to a smaller FPGA containing only the necessary resources. This approach reduces production costs, as smaller FPGAs are more affordable and consume less power. Reduced power consumption is essential for cost-sensitive and power-sensitive applications, such as IoT devices and portable electronics. This application note describes how to migrate your design from a Ti375, Ti240, Ti165, Tz325, or Tz200 in an N484 package (herein referred to as a "larger N484 FPGA"), which is commonly used for development purposes, to a smaller N484 production FPGA, such as the Ti135, Ti85, Tz100, or Tz75 (herein referred to as a "smaller N484 FPGA").



Important: After migrating to a smaller N484 FPGA, you must recalibrate the LVDS, MIPI, and DDR due to changes in the package net length. For the package net length of smaller N484 FPGAs, visit [Board Design page of the Support Center](#).

Migratable Resources

Table 1: Migratable Resource

Resource		Larger N484 FPGA	Smaller N484 FPGA	Compatible Resources
Single-Ended GPIO	HVIO VCMOS: 1.8, 2.5, 3.0, 3.3 V LVTTL: 3.0, 3.3 V	20	21	20
	HSIO LVCMOS: 1.2, 1.5, 1.8 V HSTL and SSTL (Output): 1.2, 1.35, 1.5, 1.8 V	85	85	85
	HSIO HSTL and SSTL (Input and Bidirectional): 1.2, 1.35, 1.5, 1.8 V	85	85	16
Differential GPIO	HSIO (LVDS, RSDS, mini-LVDS, Sub-LVDS, SLVS)	42	42	42
	HSIO Differential HSTL and SSTL (Output): 1.2, 1.35, 1.5, 1.8 V	85	85	85
	HSIO Differential HSTL and SSTL (Input and Bidirectional): 1.2, 1.35, 1.5, 1.8 V	85	85	16
MIPI D-PHY RX Lane	MIPI D-PHY Data Lanes	28	34	18
	MIPI D-PHY Clock Lanes	7	7	4
MIPI D-PHY Hard Block	RX	1	1	1
	TX or SSC PLL	1	1	1

Resource		Larger N484 FPGA	Smaller N484 FPGA	Compatible Resources
LPDDR4 PHY with Memory Controller	x32 DQ width	1	1	1
Global Clock or Control Signals from GPIO Pins (GCLK)		17	24	14
Fractional PLLs	PLL	9	8	8
	Reference Clock from GPIO pins (PLL_CLKIN)	12	13	9
	External Feedback I/O (PLL_EXTFB)	6	5	3
Transceiver	PCIe (Titanium FPGAs)	1xGen4	1xGen4	1xGen4
	PCIe (Topaz FPGAs)	1xGen3	1xGen3	1xGen3
	SGMII, 10GBase-KR, or PMA Direct	Up to 2	Up to 2	Up to 2
Hardened RISC-V		1	1	1

Incompatible Pin Functions

There is a mismatch in the pin functions between larger N484 FPGAs and smaller N484 FPGAs, as detailed in the table below. Please observe appropriate migration strategies for this pin to avoid hardware conflicts. If the board design needs to be compatible between both larger and smaller N484 FPGAs, the H5 package pin should be treated as reference resistor (REF_RES) pin.

Table 2: Incompatible Pin Functions

Package Pin	Larger N484 FPGA	Smaller N484 FPGA	Instruction
H5	REF_RES_4B	GPOR_132	Efinix suggests you to preserve this pin for connecting to ground through a 10 kΩ resistor of ±1% as REF_RES during board design if you do not need the extra HVIO resources available in a smaller N484 FPGA.

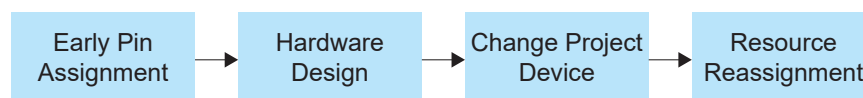


Note: If preserving the (REF_RES) pin in a smaller N484 FPGA, Efinix advises you to instantiate (GPOR_132) as input with weak pull-low in the Interface Designer to minimize pin leakage as unused pins will default to weak pull-up.

Migration Flow

Due to functional differences between the pins in larger N484 FPGAs versus smaller N484 FPGAs, Efinix recommends using the migration flow outlined below when planning to transition from a larger N484 development FPGA to a smaller N484 production FPGA.

Figure 1: Migration Flow



Early Pin Assignment

When planning for migration from a larger N484 FPGA to a smaller N484 FPGA, pay careful attention to pin compatibility. While the HVIO, MIPI D-PHY, DDR, and transceiver pins are fully compatible, some HSIO pins have functional differences. Therefore, customers should carefully plan pin assignments if they use the HSIO pins for the following:

- I/Os on banks 2B_2C and 4C
- Global clock and control network (GCLK) pins
- PLL clock input (PLL_CLKIN) and PLL external feedback (PLL_EXTFB) pins
- Input HSTL/differential HSTL and SSTL/differential SSTL
- MIPI RX lane

Input/Outputs (I/Os) on Banks 2B_2C and 4C

When using I/Os on banks 2B_2C and 4C in a larger N484 FPGA, verify that the bank voltages remain the same after migration. After migration, the 2B_2C I/Os in the larger N484 FPGA are mapped to 2A and 2B in the smaller N484 FPGA, while the 4C I/Os in the larger N484 FPGA will be mapped to 4A and 4B in the smaller N484 FPGA. Refer to the table below for detailed I/O bank migration mapping.

Table 3: I/O Bank Migration for Banks 2B_2C and _4C

Bank numbers with the same color share the same power rail.

Package Pin	Larger N484 FPGA		Smaller N484 FPGA	
	Bank Number	Pin Name	Bank Number	Pin Name
T16	2B	GPIOT_N_14	2A	GPIOT_P_00_CLK26_P
T17	2C	GPIOT_P_29	2A	GPIOT_P_01_CLK27_P
R16	2C	GPIOT_N_29	2A	GPIOT_N_01_CLK27_N
N17	2C	GPIOT_P_32	2A	GPIOT_P_02
N16	2C	GPIOT_N_32	2A	GPIOT_N_02
T19	2C	GPIOT_P_33_CLK16_P	2B	GPIOT_P_22_CLK16_P
R18	2C	GPIOT_N_33_CLK16_N	2B	GPIOT_N_22_CLK16_N
R17	2C	GPIOT_P_34_CLK17_P	2A	GPIOT_P_04_CLK31_P
P18	2C	GPIOT_N_34_CLK17_N	2A	GPIOT_N_04_CLK31_N
F1	4C	GPIOB_N_30_CDI8	4A	GPIOB_N_22
E1	4C	GPIOB_P_30_CDI9_PLLIN0	4A	GPIOB_P_22_EXTFB
J3	4C	GPIOB_N_29_CDI10	4B	GPIOB_N_16_CDI8_CLK3_N
H3	4C	GPIOB_P_29_CDI11_EXTFB	4B	GPIOB_P_16_CDI9_CLK3_P
L4	4C	GPIOB_N_26_SSU_N	4A	GPIOB_N_20_SSU_N_CLK6_N
K4	4C	GPIOB_P_26_EXTSPICLK	4A	GPIOB_P_20_EXTSPICLK_CLK6_P
H2	4C	GPIOB_N_25_CDI12	4A	GPIOB_N_18_CLK5_N
G2	4C	GPIOB_P_25_CDI13	4A	GPIOB_P_18_CLK5_P
K3	4C	GPIOB_N_24_CDI14	4B	GPIOB_N_08
K2	4C	GPIOB_P_24_CDI15	4B	GPIOB_P_08
J1	4C	GPIOB_N_23_CBSEL0	4A	GPIOB_N_19_CBSEL0
H1	4C	GPIOB_P_23_CBSEL1	4A	GPIOB_P_19_CBSEL1
M5	4C	GPIOB_N_20_CLK7_N	4B	GPIOB_N_09
L5	4C	GPIOB_P_20_CLK7_P	4B	GPIOB_P_09
L7	4C	GPIOB_N_19_TEST_N_CLK6_N	4A	GPIOB_N_17_TEST_N_CLK4_N
L6	4C	GPIOB_P_19_NSTATUS_CLK6_P	4A	GPIOB_P_17_NSTATUS_CLK4_P

Global Clock and Control Network (GCLK) Pins

Not all GCLK pins in larger N484 FPGAs are compatible those in smaller N484 FPGAs. Of the 17 GCLK pins available in larger N484 FPGAs, only 14 are compatible with the smaller N484 FPGAs. Therefore, your selection of GCLK pins is critical. Refer to the table below for compatible GCLK pins.

Table 4: Compatible GCLK Pins

Package Pin	Larger N484 FPGA		Smaller N484 FPGA	
	Bank Number	Pin Name	Bank Number	Pin Name
T19	2C	GPIOT_P_33_CLK16_P	2B	GPIOT_P_22_CLK16_P
R18	2C	GPIOT_N_33_CLK16_N	2B	GPIOT_N_22_CLK16_N
R17	2C	GPIOT_P_34_CLK17_P	2A	GPIOT_P_04_CLK31_P
P18	2C	GPIOT_N_34_CLK17_N	2A	GPIOT_N_04_CLK31_N
U22	2D	GPIOT_P_37_CLK20_P	2B	GPIOT_P_23_CLK17_P
T22	2D	GPIOT_N_37_CLK20_N	2B	GPIOT_N_23_CLK17_N
U20	2D	GPIOT_P_38_CLK21_P	2B	GPIOT_P_24_CLK18_P
T21	2D	GPIOT_N_38_CLK21_N	2B	GPIOT_N_24_CLK18_N
R21	2D	GPIOT_P_40_CLK23_P	2B	GPIOT_P_25_CLK19_P
R22	2D	GPIOT_N_40_CLK23_N	2B	GPIOT_N_25_CLK19_N
N21	TR1	GPIOR_95_CLK12	TR1	GPIOR_80_CLK12
N22	TR1	GPIOR_96_CLK13	TR1	GPIOR_81_CLK13
M8	BR0	GPIOR_142_CLK8	BR0	GPIOR_127_CLK8
K7	BR0	GPIOR_143_CLK9	BR0	GPIOR_128_CLK9
A2	4B	GPIOB_N_43_CSI_CLK10_N	4A	GPIOB_N_28_CSI_CLK11_N
A3	4B	GPIOB_P_43_CSO_CLK10_P	4A	GPIOB_P_28_CSO_CLK11_P
L7	4C	GPIOB_N_19_TEST_N_CLK6_N	4A	GPIOB_N_17_TEST_N_CLK4_N
L6	4C	GPIOB_P_19_NSTATUS_CLK6_P	4A	GPIOB_P_17_NSTATUS_CLK4_P
M3	4D	GPIOB_N_15_CDI16_CLK2_N	4B	GPIOB_N_15_CDI10_CLK2_N
M4	4D	GPIOB_P_15_CDI17_CLK2_P	4B	GPIOB_P_15_CDI11_CLK2_P
R4	4D	GPIOB_N_14_CDI18_CLK1_N	4B	GPIOB_N_14_CLK1_N
P5	4D	GPIOB_P_14_CDI19_CLK1_P	4B	GPIOB_P_14_CLK1_P
L1	4D	GPIOB_N_13_CDI20_CLK0_N	4B	GPIOB_N_13_CLK0_N
K1	4D	GPIOB_P_13_CDI21_CLK0_P	4B	GPIOB_P_13_CLK0_P

PLL_CLKIN and PLL_EXTFB Pin

Migrating the PLL_CLKIN pins is important because most designs require these pins to drive the PLL's reference clock. Of the 12 PLL_CLKIN pins in larger N484 FPGAs, only nine are compatible with the smaller N484 FPGAs. Refer to the table below for compatible PLL_CLKIN pins.

Table 5: Compatible PLL_CLKIN Pins

Package Pin	Larger N484 FPGA		Smaller N484 FPGA	
	Bank Number	Pin Name	Bank Number	Pin Name
M17	2D	GPIOT_P_50_PLLIN0	2B	GPIOT_P_20_PLLIN0
J17	2E	GPIOT_P_59_PLLIN0	2C	GPIOT_P_34_PLLIN0
L19	2E	GPIOT_P_62_PLLIN0	2C	GPIOT_P_37_CDI23_PLLIN0
M20	TR1	GPIOR_93_PLLIN1	TR1	GPIOR_78_PLLIN1
L8	BR0	GPIOR_140_PLLIN1	BR0	GPIOR_130_PLLIN1
K6	BR0	GPIOR_145_PLLIN1	BR0	GPIOR_129_PLLIN1
H9	BR3	GPIOR_165_PLLIN1	BL3	GPIOL_32_PLLIN1
L2	4D	GPIOB_P_07_CDI24_PLLIN0	4B	GPIOB_P_06_PLLIN0
R3	4D	GPIOB_P_03_PLLIN0	4B	GPIOB_P_03_PLLIN0

Additionally, if using the PLL in external I/O feedback mode, be sure to check for PLL_EXTFB pin compatibility. Without redesigning the PCB, only three PLLs support this mode. The following table shows compatible PLL_EXTFB pins.

Table 6: Compatible PLL_EXTFB Pins

Package Pin	Larger N484 FPGA		Small N484 FPGA	
	Bank Number	Pin Name	Bank Number	Pin Name
M18	2D	GPIOT_P_49_EXTFB	2B	GPIOT_P_19_EXTFB
R6	4D	GPIOB_P_06_CDI26_EXTFB	4B	GPIOB_P_07_EXTFB
N1	4D	GPIOB_P_04_CDI30_EXTFB	4B	GPIOB_P_04_EXTFB

Input HSTL/Differential HSTL and SSTL/Differential SSTL

Due to differences in VREF pin compatibility, Efnix recommends using 2D on larger N484 FPGAs for input HSTL/differential HSTL and SSTL/differential SSTL. This usage simplifies migration to a smaller N484 FPGA in the future. The tables below detail compatible VREF and input HSTL/differential HSTL and SSTL/differential SSTL.

Table 7: Compatible VREF Pins

Package Pin	Larger N484 FPGA		Smaller N484 FPGA	
	Bank Number	Pin Name	Bank Number	Pin Name
P19	2D	GPIOT_P_43	2B	GPIOT_P_18

Table 8: Compatible Input HSTL/Differential HSTL and SSTL/Differential SSTL Pins

Package Pin	Larger N484 FPGA		Smaller N484 FPGA	
	Bank Number	Pin Name	Bank Number	Pin Name
U22	2D	GPIOT_P_37_CLK20_P	2B	GPIOT_P_23_CLK17_P
T22	2D	GPIOT_N_37_CLK20_N	2B	GPIOT_N_23_CLK17_N
U20	2D	GPIOT_P_38_CLK21_P	2B	GPIOT_P_24_CLK18_P
T21	2D	GPIOT_N_38_CLK21_N	2B	GPIOT_N_24_CLK18_N
T20	2D	GPIOT_P_39_CLK22_P	2B	GPIOT_P_21
R19	2D	GPIOT_N_39_CLK22_N	2B	GPIOT_N_21
R21	2D	GPIOT_P_40_CLK23_P	2B	GPIOT_P_25_CLK19_P
R22	2D	GPIOT_N_40_CLK23_N	2B	GPIOT_N_25_CLK19_N
P20	2D	GPIOT_P_41	2B	GPIOT_P_17
P21	2D	GPIOT_N_41	2B	GPIOT_N_17
P19	2D	GPIOT_P_43	2B	GPIOT_P_18
N18	2D	GPIOT_N_43	2B	GPIOT_N_18
M18	2D	GPIOT_P_49_EXTFB	2B	GPIOT_P_19_EXTFB
M19	2D	GPIOT_N_49	2B	GPIOT_N_19
M17	2D	GPIOT_P_50_PLLIN0	2B	GPIOT_P_20_PLLIN0
L17	2D	GPIOT_N_50	2B	GPIOT_N_20

MIPI RX Lane

Unlike MIPI D-PHY RX, migrating the MIPI RX lane requires careful pin assignment planning as not all lanes are compatible with smaller N484 FPGAs. Refer to the compatibility table below for compatible MIPI RX lanes.

Table 9: Compatible MIPI RX Lanes

Package Pin	Larger N484 FPGA		Smaller N484 FPGA			
	Bank Number	Pin Name	Bank Number	Pin Name		
T17	I4	RX_DATA_P1_I4	I0	RX_DATA_P1_I0		
R16		RX_DATA_N1_I4		RX_DATA_N1_I0		
N17		RX_CLK_P_I4		RX_CLK_P_I0		
N16		RX_CLK_N_I4		RX_CLK_N_I0		
R17		RX_DATA_P5_I4		RX_DATA_P3_I0		
P18		RX_DATA_N5_I4		RX_DATA_N3_I0		
U22		I5		RX_DATA_P0_I5	I3	RX_DATA_P5_I3
T22	RX_DATA_N0_I5		RX_DATA_N5_I3			
U20	RX_DATA_P1_I5		RX_DATA_P6_I3			
T21	RX_DATA_N1_I5		RX_DATA_N6_I3			
T20	RX_CLK_P_I5		RX_CLK_P_I3			
R19	RX_CLK_N_I5		RX_CLK_N_I3			
R21	RX_DATA_P2_I5		RX_DATA_P7_I3			
R22	RX_DATA_N2_I5		RX_DATA_N7_I3			
P20	RX_DATA_P3_I5		RX_DATA_P0_I3			
P21	RX_DATA_N3_I5		RX_DATA_N0_I3			
M3	I15		RX_DATA_N6_I15	I8		RX_DATA_N6_I8
M4			RX_DATA_P6_I15			RX_DATA_P6_I8
R4		RX_DATA_N5_I15	RX_DATA_N5_I8			
P5		RX_DATA_P5_I15	RX_DATA_P5_I8			
L1		RX_DATA_N4_I15	RX_DATA_N4_I8			
K1		RX_DATA_P4_I15	RX_DATA_P4_I8			
N2		RX_CLK_N_I15	RX_CLK_N_I8			
N3		RX_CLK_P_I15	RX_CLK_P_I8			
N5		RX_DATA_N1_I15	RX_DATA_N3_I8			
N6		RX_DATA_P1_I15	RX_DATA_P3_I8			

Package Pin	Larger N484 FPGA		Smaller N484 FPGA	
	Bank Number	Pin Name	Bank Number	Pin Name
M2	I16	RX_DATA_N3_I16	I9	RX_DATA_N2_I9
L2		RX_DATA_P3_I16		RX_DATA_P2_I9
T6		RX_DATA_N2_I16		RX_DATA_N3_I9
R6		RX_DATA_P2_I16		RX_DATA_P3_I9
P3		RX_CLK_N_I16		RX_CLK_N_I9
P4		RX_CLK_P_I16		RX_CLK_P_I9
P1		RX_DATA_N1_I16		RX_DATA_N1_I9
N1		RX_DATA_P1_I16		RX_DATA_P1_I9
R2		RX_DATA_N0_I16		RX_DATA_N0_I9
R3		RX_DATA_P0_I16		RX_DATA_P0_I9

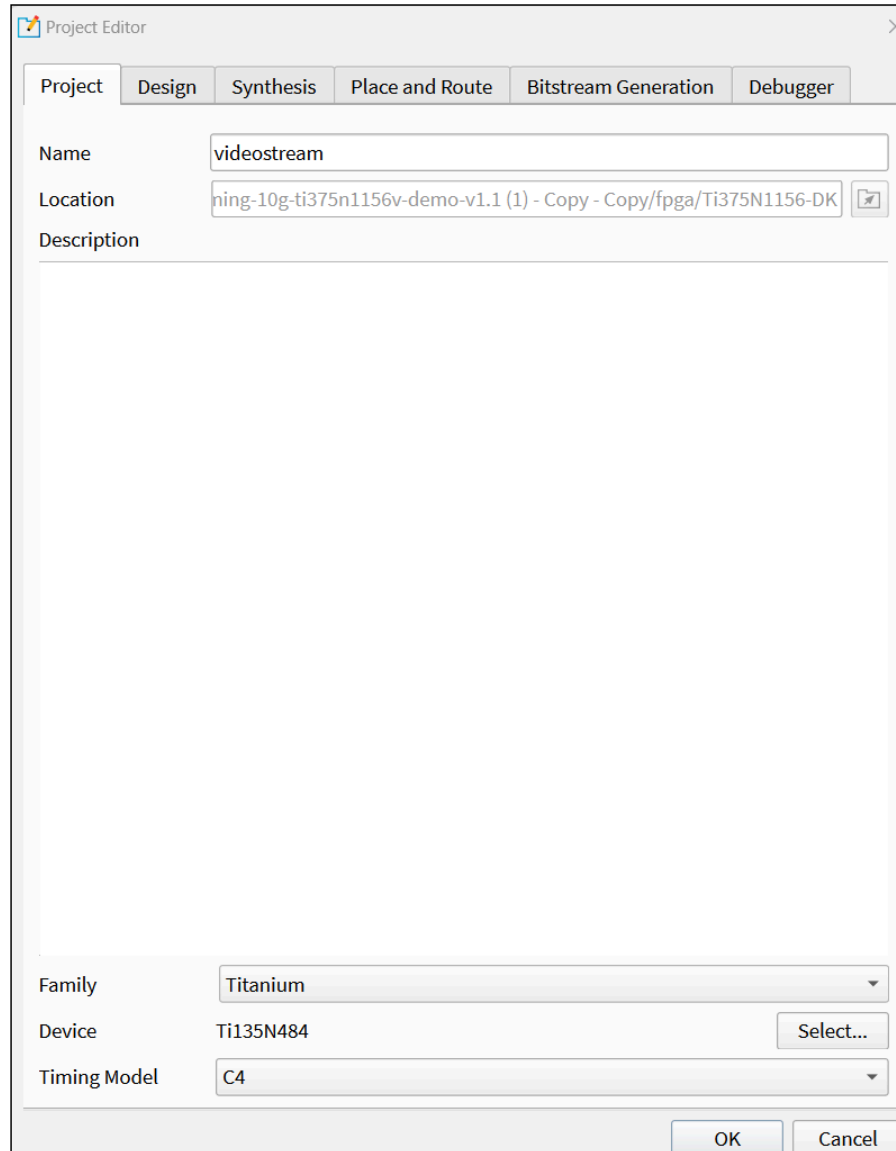
Hardware Design

After finalizing the pin assignment using the Efinity Interface Designer, you can proceed on to the hardware design phase. This stage typically involves writing the RTL code and designing the PCB layout for your project.

Change Project Device

Use the Efinity Project Editor to change the target device to one of the smaller N484 FPGAs; the Ti135N484 FPGA is shown here for example purposes.

Figure 2: Efinity Project Editor



Resource Reassignment

When you change your project to target a different FPGA/package combination, the software tries to migrate the resource assignments. If it cannot migrate the resources automatically, it launches the **Migrate Design** wizard. This wizard helps you decide how to handle the changes. The following sections show the resource assignment changes you need to make when migrating from larger N484 FPGAs to smaller ones.

GPIO

Table 10: GPIO Resource Reassignment

Package Pin	Resource	
	Larger N484 FPGA	Smaller N484 FPGA
T16	GPIOT_N_14	GPIOT_P_00_CLK26_P
T17	GPIOT_P_29	GPIOT_P_01_CLK27_P
R16	GPIOT_N_29	GPIOT_N_01_CLK27_N
N17	GPIOT_P_32	GPIOT_P_02
N16	GPIOT_N_32	GPIOT_N_02
T19	GPIOT_P_33_CLK16_P	GPIOT_P_22_CLK16_P
R18	GPIOT_N_33_CLK16_N	GPIOT_N_22_CLK16_N
R17	GPIOT_P_34_CLK17_P	GPIOT_P_04_CLK31_P
P18	GPIOT_N_34_CLK17_N	GPIOT_N_04_CLK31_N
U22	GPIOT_P_37_CLK20_P	GPIOT_P_23_CLK17_P
T22	GPIOT_N_37_CLK20_N	GPIOT_N_23_CLK17_N
U20	GPIOT_P_38_CLK21_P	GPIOT_P_24_CLK18_P
T21	GPIOT_N_38_CLK21_N	GPIOT_N_24_CLK18_N
T20	GPIOT_P_39_CLK22_P	GPIOT_P_21
R19	GPIOT_N_39_CLK22_N	GPIOT_N_21
R21	GPIOT_P_40_CLK23_P	GPIOT_P_25_CLK19_P
R22	GPIOT_N_40_CLK23_N	GPIOT_N_25_CLK19_N
P20	GPIOT_P_41	GPIOT_P_17
P21	GPIOT_N_41	GPIOT_N_17
P19	GPIOT_P_43	GPIOT_P_18
N18	GPIOT_N_43	GPIOT_N_18
M18	GPIOT_P_49_EXTFB	GPIOT_P_19_EXTFB
M19	GPIOT_N_49	GPIOT_N_19
M17	GPIOT_P_50_PLLIN0	GPIOT_P_20_PLLIN0
L17	GPIOT_N_50	GPIOT_N_20
K16	GPIOT_P_57	GPIOT_P_39_CLK15_P
K17	GPIOT_N_57	GPIOT_N_39_CLK15_N
J17	GPIOT_P_59_PLLIN0	GPIOT_P_34_PLLIN0

Package Pin	Resource	
	Larger N484 FPGA	Smaller N484 FPGA
K18	GPIOT_N_59	GPIOT_N_34
L19	GPIOT_P_62_PLLIN0	GPIOT_P_37_CDI23_PLLIN0
L20	GPIOT_N_62	GPIOT_N_37_CDI22
J19	GPIOT_P_64_CLK15_P	GPIOT_P_35
K19	GPIOT_N_64_CLK15_N	GPIOT_N_35
M20	GPIOR_93_PLLIN1	GPIOR_78_PLLIN1
N20	GPIOR_94	GPIOR_79
N21	GPIOR_95_CLK12	GPIOR_80_CLK12
N22	GPIOR_96_CLK13	GPIOR_81_CLK13
M22	GPIOR_97	GPIOR_82
L21	GPIOR_98	GPIOR_83
L22	GPIOR_99	GPIOR_84
L8	GPIOR_140_PLLIN1	GPIOR_130_PLLIN1
K8	GPIOR_141	GPIOR_125
M8	GPIOR_142_CLK8	GPIOR_127_CLK8
K7	GPIOR_143_CLK9	GPIOR_128_CLK9
J6	GPIOR_144_PERST_Q2_N	GPIOR_131_PERST_Q0_N
K6	GPIOR_145_PLLIN1	GPIOR_129_PLLIN1
H9	GPIOR_165_PLLIN1	GPIOL_32_PLLIN1
H6	GPIOR_166	GPIOL_27_CLK25
G6	GPIOR_167	GPIOL_28
H7	GPIOR_168	GPIOL_31
H8	GPIOR_169	GPIOL_33
F5	GPIOR_170	GPIOL_34_PLLIN1
F4	GPIOR_171	GPIOL_26_CLK24
A2	GPIOB_N_43_CSI_CLK10_N	GPIOB_N_28_CSI_CLK11_N
A3	GPIOB_P_43_CSO_CLK10_P	GPIOB_P_28_CSO_CLK11_P
B1	GPIOB_N_41	GPIOB_N_21_CLK7_N
B2	GPIOB_P_41	GPIOB_P_21_CLK7_P
J4	GPIOB_N_40_CDI0	GPIOB_N_27_CDI0_CLK10_N
J5	GPIOB_P_40_CDI1_EXTFB	GPIOB_P_27_CDI1_CLK10_P
G3	GPIOB_N_39_CDI2	GPIOB_N_26_CDI2
G4	GPIOB_P_39_CCK_PLLIN0	GPIOB_P_26_CCK
C1	GPIOB_N_38_SSL_N	GPIOB_N_25_SSL_N
C2	GPIOB_P_38_CDI3	GPIOB_P_25_CDI3_PLLIN0
F2	GPIOB_N_37_CDI4	GPIOB_N_24_CDI4
F3	GPIOB_P_37_CDI5	GPIOB_P_24_CDI5_EXTFB

Package Pin	Resource	
	Larger N484 FPGA	Smaller N484 FPGA
D2	GPIOB_N_36_CDI6	GPIOB_N_23_CDI6
E2	GPIOB_P_36_CDI7	GPIOB_P_23_CDI7_PLLIN0
F1	GPIOB_N_30_CDI8	GPIOB_N_22
E1	GPIOB_P_30_CDI9_PLLIN0	GPIOB_P_22_EXTFB
J3	GPIOB_N_29_CDI10	GPIOB_N_16_CDI8_CLK3_N
H3	GPIOB_P_29_CDI11_EXTFB	GPIOB_P_16_CDI9_CLK3_P
L4	GPIOB_N_26_SSU_N	GPIOB_N_20_SSU_N_CLK6_N
K4	GPIOB_P_26_EXTSPICLK	GPIOB_P_20_EXTSPICLK_CLK6_P
H2	GPIOB_N_25_CDI12	GPIOB_N_18_CLK5_N
G2	GPIOB_P_25_CDI13	GPIOB_P_18_CLK5_P
K3	GPIOB_N_24_CDI14	GPIOB_N_08
K2	GPIOB_P_24_CDI15	GPIOB_P_08
J1	GPIOB_N_23_CBSEL0	GPIOB_N_19_CBSEL0
H1	GPIOB_P_23_CBSEL1	GPIOB_P_19_CBSEL1
M5	GPIOB_N_20_CLK7_N	GPIOB_N_09
L5	GPIOB_P_20_CLK7_P	GPIOB_P_09
L7	GPIOB_N_19_TEST_N_CLK6_N	GPIOB_N_17_TEST_N_CLK4_N
L6	GPIOB_P_19_NSTATUS_CLK6_P	GPIOB_P_17_NSTATUS_CLK4_P
M3	GPIOB_N_15_CDI16_CLK2_N	GPIOB_N_15_CDI10_CLK2_N
M4	GPIOB_P_15_CDI17_CLK2_P	GPIOB_P_15_CDI11_CLK2_P
R4	GPIOB_N_14_CDI18_CLK1_N	GPIOB_N_14_CLK1_N
P5	GPIOB_P_14_CDI19_CLK1_P	GPIOB_P_14_CLK1_P
L1	GPIOB_N_13_CDI20_CLK0_N	GPIOB_N_13_CLK0_N
K1	GPIOB_P_13_CDI21_CLK0_P	GPIOB_P_13_CLK0_P
N2	GPIOB_N_12	GPIOB_N_12_CDI12
N3	GPIOB_P_12	GPIOB_P_12_CDI13
N5	GPIOB_N_09	GPIOB_N_11_CDI14
N6	GPIOB_P_09	GPIOB_P_11_CDI15
P6	GPIOB_N_08	GPIOB_N_00
N7	GPIOB_P_08_CDI22_EXTFB	GPIOB_P_00_PLLIN0
M2	GPIOB_N_07_CDI23	GPIOB_N_06_CDI18
L2	GPIOB_P_07_CDI24_PLLIN0	GPIOB_P_06_PLLIN0
T6	GPIOB_N_06_CDI25	GPIOB_N_07
R6	GPIOB_P_06_CDI26_EXTFB	GPIOB_P_07_EXTFB
P3	GPIOB_N_05_CDI27	GPIOB_N_05
P4	GPIOB_P_05_CDI28_PLLIN0	GPIOB_P_05
P1	GPIOB_N_04_CDI29	GPIOB_N_04

Package Pin	Resource	
	Larger N484 FPGA	Smaller N484 FPGA
N1	GPIOB_P_04_CDI30_EXTFB	GPIOB_P_04_EXTFB
R2	GPIOB_N_03_CDI31	GPIOB_N_03
R3	GPIOB_P_03_PLLIN0	GPIOB_P_03_PLLIN0

LVDS/SLVS and MIPI Lane

Table 11: LVDS/SLVS and MIPI Lane Resource Reassignment

Package Pin	Resource	
	Larger N484 FPGA	Smaller N484 FPGA
T17	GPIOT_PN_29	GPIOT_PN_01
R16		
N17	GPIOT_PN_32	GPIOT_PN_02
N16		
T19	GPIOT_PN_33	GPIOT_PN_22
R18		
R17	GPIOT_PN_34	GPIOT_PN_04
P18		
U22	GPIOT_PN_37	GPIOT_PN_23
T22		
U20	GPIOT_PN_38	GPIOT_PN_24
T21		
T20	GPIOT_PN_39	GPIOT_PN_21
R19		
R21	GPIOT_PN_40	GPIOT_PN_25
R22		
P20	GPIOT_PN_41	GPIOT_PN_17
P21		
P19	GPIOT_PN_43	GPIOT_PN_18
N18		
M18	GPIOT_PN_49	GPIOT_PN_19
M19		
M17	GPIOT_PN_50	GPIOT_PN_20
L17		
K16	GPIOT_PN_57	GPIOT_PN_39
K17		
J17	GPIOT_PN_59	GPIOT_PN_34
K18		

Package Pin	Resource	
	Larger N484 FPGA	Smaller N484 FPGA
L19	GPIOT_PN_62	GPIOT_PN_37
L20		
J19	GPIOT_PN_64	GPIOT_PN_35
K19		
A2	GPIOB_PN_43	GPIOB_PN_28
A3		
B1	GPIOB_PN_41	GPIOB_PN_21
B2		
J4	GPIOB_PN_40	GPIOB_PN_27
J5		
G3	GPIOB_PN_39	GPIOB_PN_26
G4		
C1	GPIOB_PN_38	GPIOB_PN_25
C2		
F2	GPIOB_PN_37	GPIOB_PN_24
F3		
D2	GPIOB_PN_36	GPIOB_PN_23
E2		
F1	GPIOB_PN_30	GPIOB_PN_22
E1		
J3	GPIOB_PN_29	GPIOB_PN_16
H3		
L4	GPIOB_PN_26	GPIOB_PN_20
K4		
H2	GPIOB_PN_25	GPIOB_PN_18
G2		
K3	GPIOB_PN_24	GPIOB_PN_08
K2		
J1	GPIOB_PN_23	GPIOB_PN_19
H1		
M5	GPIOB_PN_20	GPIOB_PN_09
L5		
L7	GPIOB_PN_19	GPIOB_PN_17
L6		
M3	GPIOB_PN_15	GPIOB_PN_15
M4		
R4	GPIOB_PN_14	GPIOB_PN_14

Package Pin	Resource	
	Larger N484 FPGA	Smaller N484 FPGA
P5		
L1	GPIOB_PN_13	GPIOB_PN_13
K1		
N2	GPIOB_PN_12	GPIOB_PN_12
N3		
N5	GPIOB_PN_09	GPIOB_PN_11
N6		
P6	GPIOB_PN_08	GPIOB_PN_00
N7		
M2	GPIOB_PN_07	GPIOB_PN_06
L2		
T6	GPIOB_PN_06	GPIOB_PN_07
R6		
P3	GPIOB_PN_05	GPIOB_PN_05
P4		
P1	GPIOB_PN_04	GPIOB_PN_04
N1		
R2	GPIOB_PN_03	GPIOB_PN_03
R3		

PLL

Table 12: PLL Resource Reassignment

PLL Resource	
Smaller N484 FPGA	Larger N484 FPGA
PLL_TR0	PLL_TR0 ⁽¹⁾
PLL_TR1	PLL_TR1 ⁽¹⁾
PLL_TR2	PLL_TR2 ⁽¹⁾
PLL_BR0	PLL_BR1 ⁽¹⁾
PLL_BR1	PLL_BR0 ⁽¹⁾
PLL_BR2	PLL_BL1 ⁽¹⁾
PLL_BL0	PLL_BL1 ⁽¹⁾
PLL_BL1	PLL_BL0 ⁽²⁾
PLL_BL2	PLL_BL2 ⁽¹⁾

⁽¹⁾ Chosen as the PLL resource reassignment due to PLL_CLKIN compatibility.

⁽²⁾ Chosen as the PLL resource reassignment because there is no compatible PLL_CLKIN.

*MIPI DPHY TX***Table 13: MIPI D-PHY TX Resource Reassignment**

MIPI TX Resource	
Smaller N484 FPGA	Larger N484 FPGA
MIPI_TX1	MIPI_TX2

*MIPI DPHY RX***Table 14: MIPI D-PHY RX Resource Reassignment**

MIPI RX Resource	
Smaller N484 FPGA	Larger N484 FPGA
MIPI_RX1	MIPI_RX2

*DDR***Table 15: DDR Resource Reassignment**

DDR Resource	
Smaller N484 FPGA	Larger N484 FPGA
DDR_0	DDR_0

*PLL SSC***Table 16: PLL SSC Resource Reassignment**

PLL SSC Resource	
Smaller N484 FPGA	Larger N484 FPGA
MIPI_TX1	MIPI_TX2

*PCI Express***Table 17: PCI Express Resource Reassignment**

PCI Express Resource	
Smaller N484 FPGA	Larger N484 FPGA
QUAD_0	QUAD_2

*Ethernet XGMII***Table 18: Ethernet XGMII Resource Reassignment**

Ethernet XGMII Resource	
Smaller N484 FPGA	Larger N484 FPGA
Q0_LN0	Q2_LN0

Ethernet XGMII Resource	
Smaller N484 FPGA	Larger N484 FPGA
Q0_LN1	Q2_LN1
Q0_LN2	Q2_LN2
Q0_LN3	Q2_LN3
Q1_LN0	Q3_LN0
Q1_LN1	Q3_LN1
Q1_LN2	Q3_LN2
Q1_LN3	Q3_LN3

PMA Direct

Table 19: PMA Direct Resource Reassignment

PMA Direct Resource	
Smaller N484 FPGA	Larger N484 FPGA
Q0_LN0	Q2_LN0
Q0_LN1	Q2_LN1
Q0_LN2	Q2_LN2
Q0_LN3	Q2_LN3
Q1_LN0	Q3_LN0
Q1_LN1	Q3_LN1
Q1_LN2	Q3_LN2
Q1_LN3	Q3_LN3

Revision History

Date	Version	Description
November 2025	1.3	Expanded coverage to all Titanium and Topaz devices with N484 packages. (DOC-2774)
May 2025	1.2	Added Incompatible Pin Functions on page 4. (DOC-2519) Updated Migratable Resources on page 3. (DOC-2519)
March 2025	1.1	Fix typo MIPI DPHY TX on page 19. (DOC-2450) Fix typo MIPI DPHY RX on page 19. (DOC-2450) Fix typo PLL SSC on page 19. (DOC-2450) Fix typo PCI Express on page 19. (DOC-2450) Fix typo Ethernet XGMII on page 19. (DOC-2450) Fix typo PMA Direct on page 20. (DOC-2450)
February 2025	1.0	Initial release.