



# AN 065: Using the Topaz Power Estimator

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# Introduction

Designing low-power systems has become increasingly important. Battery-powered, handheld, IoT, and mobile applications are obvious power-sensitive systems. However, even in power-hungry systems, just a few percent of power savings can translate into significant operating cost reductions.

Each Topaz FPGA has its own unique power profile. Therefore, Efinix® provides a power estimator for each family member. These tools are Excel spreadsheets with macros. You can select the desired Topaz FPGA power estimator file, add information about your design, and the estimator calculates the projected power consumption. However, you need a license to obtain the **Power Estimator** Excel file from [Efinix® Support Center](#).



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**Note:**

- The power estimators are just that - an estimate. They are intended to help guide your decision-making process as you pick an FPGA and plan your design. You should verify the actual power consumption in your system.
  - Refer to the respective [datasheet](#) in the Support Center for the availability of device interface (e.g., package and device-specific interface).
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## Total Tab

The Total tab is where you provide high-level information about your target FPGA and your system's thermal profile. It also displays power estimation summaries. Spreadsheet cells with a blue background are either static or calculated. White cells are for user input.

## Device Settings

Enter data about the FPGA you want to use in the Device Settings table. Different FPGAs consume different amounts of power for the same design. For example, a larger FPGA consumes more power than a smaller one.



**Note:** Refer to the maximum condition for power budgeting. The default power settings assume a typical usage scenario. In worst case power usage scenarios, however, power budgeting may be preferable.

*Table 1: Device Settings*

Option	Choices	Notes
Package	Dependent on the FPGA	The package size affects the thermal resistance. The number of tabs in the spreadsheet changes based on the package you choose.
Speed Grade	Commercial, Industrial, Automotive	Commercial is 0 to 85 °C. Industrial is -40 to 100 °C. Automotive is -40 to 125 °C.
Condition	Typical, Maximum	Choose the static leakage power to mimic. Typical corresponds to the most frequent condition. Maximum corresponds to the worst case leakage condition.

## Thermal Profile

The estimator performs thermal analysis based on the FPGA you choose, the ambient temperature, and the airflow. The FPGA itself is a heat source, so the ambient temperature while it is operating, and the amount of cooling, if any, affects the overall power consumption.

The estimator calculates the effective  $\Theta_{JA}$  and junction temperature based on your selections.

**Table 2: Thermal Profile**

Option	Choices	Notes
Ambient Temperature (°C)	User defined.	Enter the ambient temperature under which you expect your system to operate. Efinix recommends that you do not operate the FPGA at temperatures higher than the shown maximum ambient temperature.
Airflow	0.0 m/s, 1.0 m/s, 2.0 m/s	Default value is 0.0 m/s which is still air.
Board Thermal Profile	JEDEC (2s2p)	This is the profile that Efinix has modeled.
Effective Theta-JA (°C/W)	Default	Only default value is available.

The **Notes** field shows warning messages if the junction temperature exceeds the user selected operating temperature range or if there is a thermal runaway causing the leakage power to never converge.

## Power Supply Summary

The Power Supply Summary table shows the estimated current consumption in mA for each voltage domain for the resource utilization you specify. This summary includes static and dynamic power consumption. These values help you to determine the specifications for the power regulator to use on your board.



**Note:** Transient current is unpreventable during switching activities; you will need to keep this in mind when setting up the voltage regulator to manage the transient current.

## Block Power Summary

The Block Power Summary table shows the static and dynamic power consumption totals from the other tabs in the worksheet.

The static power shows device leakage power and design static power. Device leakage power represents transistor leakage power following power up. Design static power is a product of the power consumed when device is correctly configured, but there is no switching activity.

The dynamic power is an indicator the power consumed due to the user's resource utilization during switching activity.

The total power shows the static power + dynamic power.

## MIPI Estimate Core Power

The MIPI Estimate Core Power shows the estimation of the power consumption of MIPI implementation in your design in mW. The MIPI Estimate Core Power value is calculated from values inserted in the HSIO Configured as MIPI Lanes table of the GPIO tab.

- If you already have a design using HSIO as MIPI lanes, you get resources from the synthesis report and enter it in the HSIO Configured as MIPI Lanes table of the GPIO tab. In this scenario, the estimator includes the MIPI Estimate Core Power value in the Total Power value.
- If you have not created a design yet and are just exploring power options, include the planned HSIO as MIPI lane usage in the HSIO Configured as MIPI Lanes table of the GPIO tab. In this scenario, the estimator does not include the MIPI Estimate Core Power value in the Total Power value. To get the actual total power including MIPI, add MIPI Estimate Core Power to the Total Power.

## Logic, Memory, and DSP Tabs

Your design will have at least one, and probably more, modules. To get a better power estimation, list the modules, their clock frequency, eXchangeable Logic and Routing (XLR) cells, number of memory blocks, and number of DSP on these tabs.

The estimation is based on the resources running with respective frequencies. the total number of resources should matched with the number of resources in `<project>.pnr.rpt`.



**Note:** XLRs can be used in different combinations such as logic, logic with flip-flop, adder, adder with flip-flop, flip-flop, SRL8, SRL8 with flip-flop.

If you already have an Efinity design, you can obtain this data from the Module Resource Usage Distribution Estimates section in the `<project>.map.rpt` file.

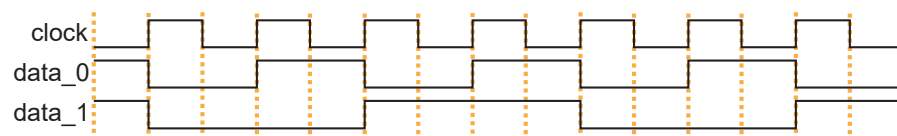
**Tip:** Click on the column heading to view pop-up help.

## About the Activity Factor

Activity Factor (AF) represents the average toggling rate of resources over a set period, represented as a percentage unit. An accurate AF is crucial for the accurate estimation of power consumption. Accurately determining AF, however, can be difficult early in the design cycle. Moreover, some applications are dependent upon input from other devices in the system. Therefore, certain assumptions are made with regard to which toggling instants are evenly distributed across different signals. The following guidelines can help you to determine the AF:

### Figure 1: Example Activity Waveform

This figure shows one clock signal and two data signals. The data\_0 signal toggles during each clock cycle, which is equivalent to an AF of 100%. data\_0 also toggles at half of the clock frequency. The data\_1 signal toggles once in every two cycles, which is equivalent to an AF of 50%.



**Note:** The default AF is 12.5% and is based on a 16-bit counter. Be aware that this AF is a summary figure that represents a set of assumptions about the rate of signalling. Nevertheless, the precise signalling pattern may differ and lead to differences in power consumption.

# Clock Tab

Power consumption is strongly correlated to the clock usage. On this tab you enter the clocks, their frequency, and the flip-flops.

If you already have an Efinity design, you can refer to the **Clock Load Distribution Report** in the `<project>.map.rpt` for the clock domain in the resource utilization section.



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**Note:** The resources from the Debugger Auto Instantiation are not included in the **Clock Load Distribution Report** of the `<project>.map.rpt`.

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# GPIO Tab

Topaz I/O pins support several I/O standards. You use this tab to summarize how many input, output, and inout (bidirectional) pins your design uses.

**Table 3: GPIO Tab Parameters**

Input Parameter	Description
I/O Standard	Currently available standards include: 1.8V LVCMOS, 2.5V LVCMOS, 3.3 LVCMOS, and 3.3 LVTTTL.
Number of input	Only applicable for LVDS RX only in pairs as the power consumption for number of input pins for other I/O standards are negligible.
Number of output	Applicable for all I/O standards. LVDS TX is in pairs and other I/O standards in number of pins. Example: Insert 1 for 1 pair of LVDS.
Number of inout (bidirectional)	Applicable for all I/O standards except LVDS in number of pins.
Date Rate	Applicable for all I/O standard except LVDS. Two options are available, SDR for single data rate, DDR for double data rate. Double data rate I/O pins are indicated with mode as DDIO in <b>&lt;project&gt;.pt.rpt.</b>
Clock Frequency	This field refers to the clock domain for the pin(s). The clock frequency is used by the signal.
Load	For output and inout pins, this field is for the pin loading (in pF). The value is the total load, including die capacitance, package capacitance, and board (off chip) capacitance. For general estimation, the sum of die and package capacitance is approximately 1 - 2 pF; can use 2 pF to be more conservative. If your off-chip capacitance is 10 pF, use 12 pF (i.e., 2 + 10) in the load cell.
Output Enable	The field is for the average percentage of time that the output and inout pins are enabled. The default is 100%.
AF	Refer to <b>About the Activity Factor</b> on page 7.

## HSIO Configured as MIPI Lanes

Topaz HSIO can be configured as MIPI TX or RX lanes. You use this tab to summarize how many input and output lanes your design uses. The estimator estimates the I/O power, core power and total power for each lane.

Each row represents one MIPI channel. Enter the modules, number of MIPI lanes, their mode, data rate, active factor, percentage of time the lane is in high-speed (HS) mode.

See [About the Activity Factor](#) on page 7 for information about the active factor.

## HSIO Configured as LVDS

Topaz HSIO can be configured as LVDS. There are programmable output differential, VOD, and output pre-emphasis. You are required to input the number of pairs, either TX or RX, along with that data rate (i.e., Mbps). The AF defaults to 50%.



**Learn more:** See [About the Activity Factor](#) on page 7 for information about the AF.



**Note:** Half-rate and full-rate modes have almost the same power consumption.

## PLL Tab

The PLL tab captures data about the PLLs your design uses. Enter the output frequency and VCO frequency for each PLL.

**Tip:** To save on power consumption, you can reduce the number of PLLs used by grouping all the clock outputs.

*Table 4: Frequency Settings*

Setting	Description
Output Clock Frequency (MHz)	In this column, insert the highest value of the output clock frequency. For example, if you have three PLL output clocks, 10 MHz, 20 MHz, and 50 MHz, use the <b>50</b> . Valid values are 0.1342 to 1000, where 0 represents no clock output.
VCO Frequency (MHz)	Insert a number between 2200 and 5500.

## MIPI Tab

The MIPI tab estimates the power consumption from the MIPI D-PHY block, by specifying the following parameters based on your implementation:

- *Transmission mode*—TX or RX
- *Data rate*—Refer to the [datasheet](#) for the MIPI D-PHY block maximum data rate.

## LPDDR4 Tab

The DDR tab contains data about the DDR interface and specifies the following:

- *DDR type*—LPDDR4, LPDDR4x
- *DQ width*—x16 or x32, the choice varies based on the FPGA and package you choose.
- *Data rate*—Refer to [datasheet](#) for the DRAM interface maximum data rate.
- *Percentage of time in read mode and write mode*—Indicate the average time portion of read and write in certain period including the time portion of period in idle state. Percentage of time in read mode (%) + percentage of time in write mode (%) + percentage of time in idle mode (%) = 100%.

## RISC-V Tab

The hardened RISC-V block<sup>(1)</sup> has four CPUs with dedicated FPU and custom instructions. Refer to the [Topaz Selector Guide](#) for devices with hardened RISC-V block support. FPGAs only.

- *Condition*—Can be disabled or used to estimate *static*, *idle*, or *running* conditions.
- *System clock*—System clock frequency, refer to [datasheet](#) for the maximum frequency.
- *Load*—Default is 50% for typical application usage. Efinix recommends that you set the load to 100% if you intend to compare your Topaz board with another FPGA using the Dhrystone benchmarking tool. Setting the load to 100% should provide for a more accurate 1:1 comparison of power consumption.

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<sup>(1)</sup> Preliminary

## Transceiver Tab

The Transceiver tab<sup>(2)</sup> estimates the power consumption for a high-speed transceiver interface. Refer to the [Topaz Selector Guide](#) for devices with transceiver support. It supports multi-protocol, including a full-duplex transceiver that supports data rates from 1.25 Gbps to 16 Gbps.

- *Resources*—Choose between QUAD\_0, QUAD\_1, QUAD\_2, or QUAD\_3. Be aware that some devices might have only QUAD\_0 and QUAD\_1, depending upon the number of transceivers allowed in the device.
- *Protocol*—Refer to [datasheet](#) for the supported protocols.
- *Data Rate (Gbps) per lane*—Select the available data rate. For PCIe, choose the generation being used.
- *Lane Count*—Number of lanes.
- *Mode*—Functions as either a transceiver, transmitter, or a receiver.
- *LP/HP*—Low-power or high-performance.

## Revision History

*Table 5: Revision History*

Date	Version	Description
December 2024	1.0	Initial release.

<sup>(2)</sup> Preliminary