



# AN 063: High-Speed Transceiver Design Guidelines

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# Introduction

Both Titanium and Topaz transceivers consist of a physical medium attachment (PMA) and a physical coding sublayer (PCS). The PMA connects the FPGA to the lane, generates the required clocks, and converts the data from parallel to serial or serial to parallel. The PCS contains the digital processing interface between the PMA and the FPGA fabric. The PCS supports SGMII, 10GBase-KR, and up to PCIe® Gen4, as well as PMA Direct.

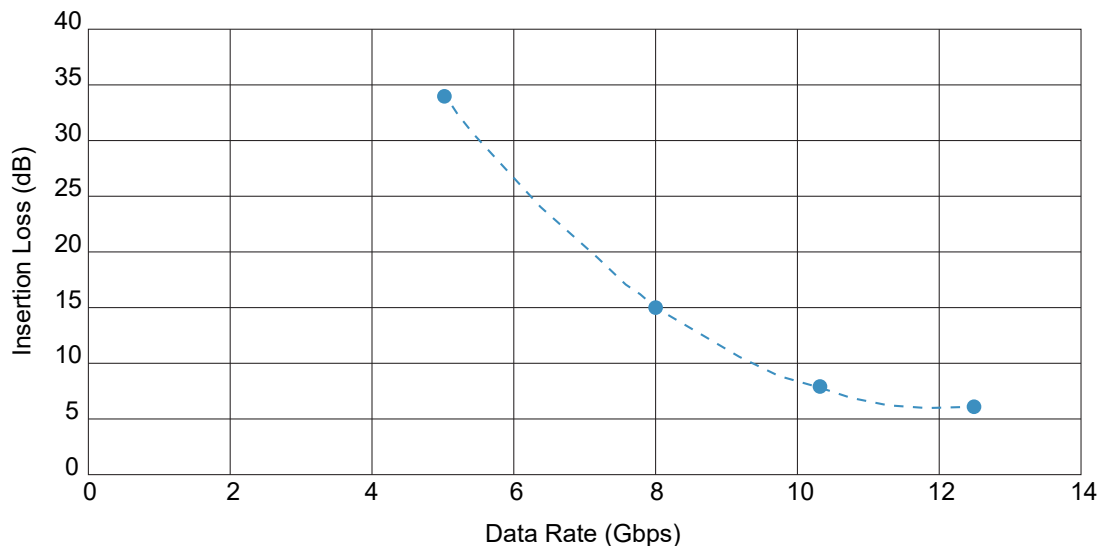
The transceivers support up to Gen4 x4, which is equivalent to a 16 Gbps lane rate or up to 64 Gbps link bandwidth. Therefore, proper hardware design is essential to ensure reliable high-speed data transmission. These guidelines provide comprehensive guidance regarding schematic-level design considerations and PCB layout guidelines for high-speed transceivers under different modes of operation.

## Circuit Design Considerations

### PMA Direct

For PMA Direct PHY operating in 20-bit or 40-bit data width mode, refer to the following graph on the maximum channel insertion loss allowed for the RX at the respective data rates.

Figure 1: 20b PHY RX Channel Loss Against Data Rate



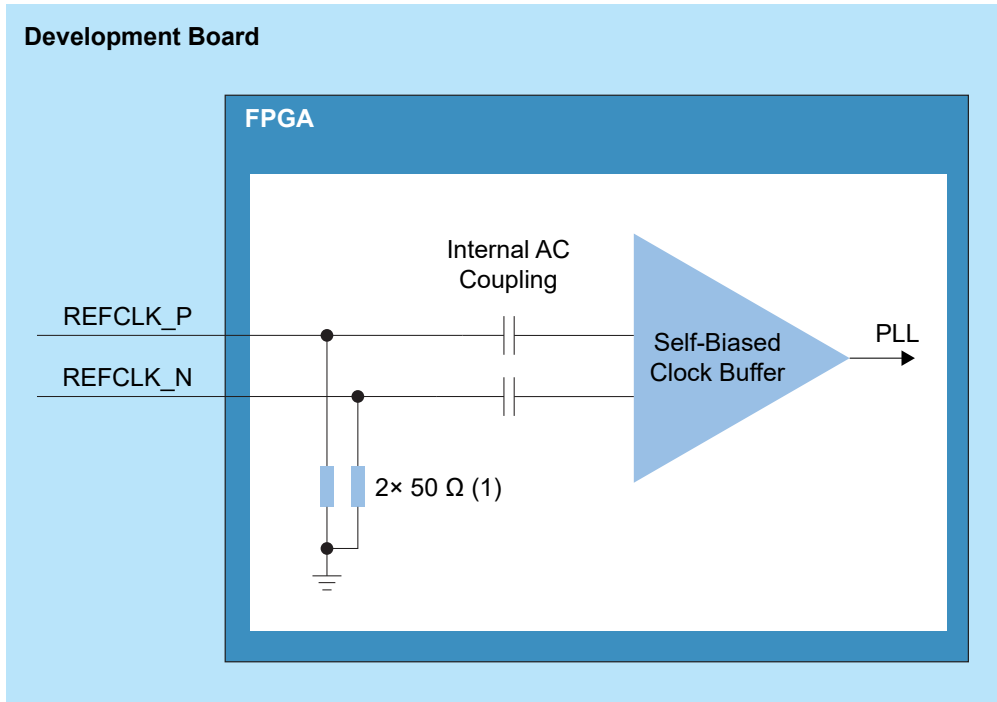
For PMA Direct PHY operating in either 32-bit or 64-bit data width modes, the maximum channel insertion loss allowed for RX is 25 dB across different data rates.

At 6.25 GHz (for 12.5 Gbps data rate), the insertion loss estimates below are based on the PCB material:

- M6: ~ 0.5 dB/inch
- FR4: ~ 1 dB/inch

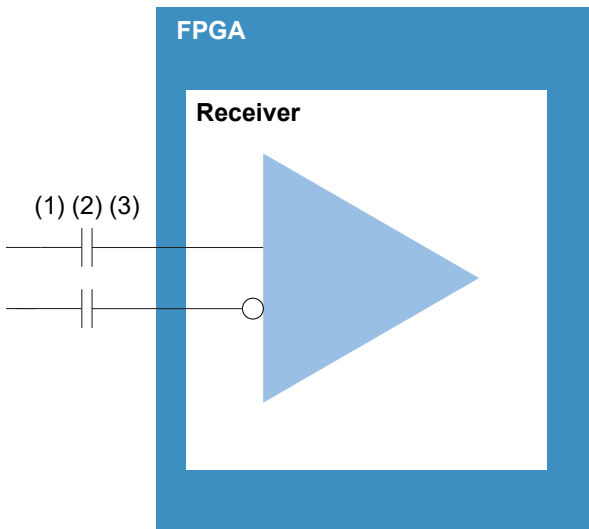
The following diagrams illustrate the AC coupling requirements associated with PMA Direct PHY.

Figure 2: Internal AC Coupling



**Note:** (1) You can turn termination on or off in the Interface Designer.

Figure 3: External RX Path



**Notes:**

- (1) Recommended capacitance: 0.1–0.22 uF.
- (2) Recommended package: 0201.
- (3) DC coupling is not supported.

## 10GBASE-R/KR

Local Area Networks (LANs) conforming to the IEEE 802.3-2012 Ethernet Standard rely on optical modules, routers, and servers corresponding to the 10GBase-R standard. The electrical backplane, on the other hand, comprises a transmission medium corresponding to the 10GBase-KR standard.

The physical 10GBase-R/KR layer includes the Physical Medium Dependent (PMD), Physical Medium Attachment (PMA), and Physical Coding Sublayer (PCS), which respectively comprise the physical connection, receive equalization/transmit equalization, receive clock recovery, parallel signal serialization/high-speed serial signal deserialization, and 64b/66b encoding and decoding. Because 10G uses 64b/66b encoding, the actual rate at which 10 Gbps data is transmitted over the medium after encoding is 10.3125 Gbps (i.e.,  $10 \text{ Gbps} \times 66 \div 64 = 10.3125 \text{ Gbps}$ ).

Therefore, the 10GBase-R/KR interface operates at a clock frequency of:  $10312.5 \div 66 = 156.25 \text{ MHz}$ .

### 10G SFP+ Interface

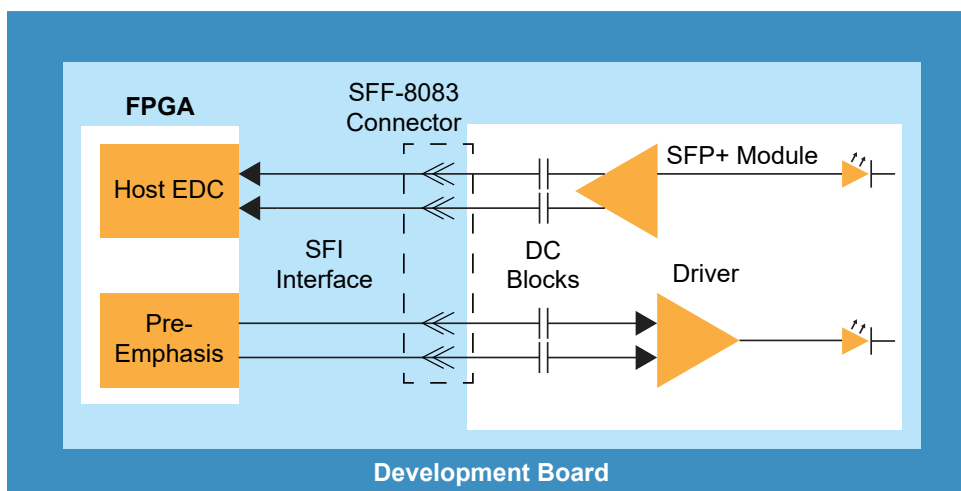
The 10G SFP+ optical module is an Enhanced Small Form-factor Pluggable (SFP+) hot-swappable optical transceiver. It is commonly used in 10 Gbps applications, such as SONET/SDH, Fiber Channel, and 10 Gigabit Ethernet. For Titanium and Topaz boards, when configured as 10GBase-R in KR mode, the high-speed transceiver interface can work with an external 10G SFP+ optical module. An example connection can be found on the Titanium Ti375 N1156 Development Board.

Because the 10G SFP+ interface is widely used, the following section uses the 10G SFP+ interface as an example to introduce the 10G transceiver interface design.

The SFP+ interface is mainly divided into two parts: host and module. The host is the part of the SFP+ optical module interface. The module itself does not consist of CDR circuits. Therefore, dimension and power consumption can be minimized.

The electrical interface connecting the FPGA transceiver interface on the host side and the SFP+ optical module is referred to as a SerDes Framer Interface (SFI). This SFI electrical interface is based on high-speed, low-voltage AC coupling logic. The nominal differential impedance is  $100 \Omega$ , as shown in the following figure.

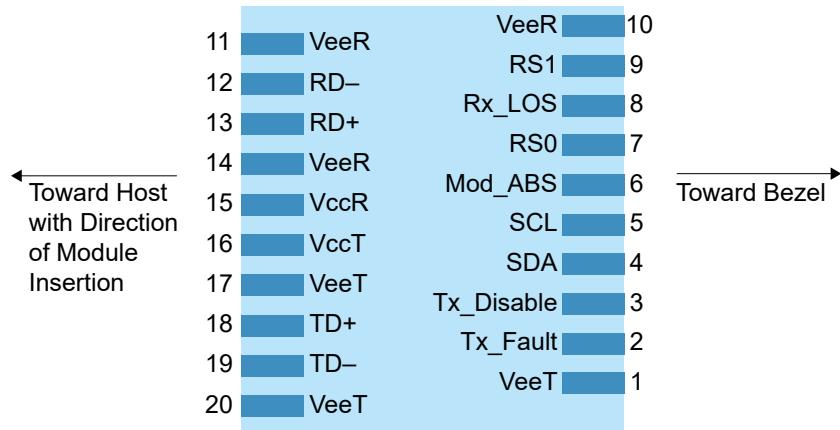
Figure 4: SFP+ Interface Block Diagram



## 10G SFP+ Interface Pinout Description

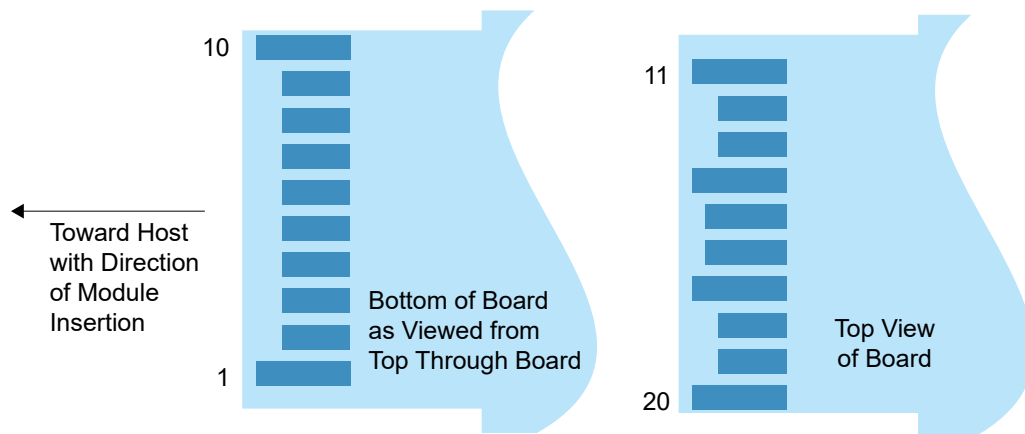
The following figure is a schematic diagram of the SFP+ interface signal on the host side, which corresponds to the 20-pin optical interface connector.

Figure 5: Host PCB SFP+ Pin Assignment



The following figure shows the pins on the side of the SFP+ optical module, which corresponds to the edge card connector of the optical module.

Figure 6: SFP+ Module Pin Assignment



The following table describes the pin assignment of the SFP+ interface:

Table 1: SFP+ Module and Host Electrical Contact Definition

Pin #	Signal Name	Logic Level	Description
1	VeeT		Module Transmitter Ground.
2	TX_Fault	LVTTL-O	Module Transmitter Fault. Open-drain output, which needs to be pulled up to VCC on the host side to indicate an error in the SFP+ module sending.
3	TX_Disable	LVTTL-I	Transmitter Disable. Turns off transmitter laser output. Required connection to FPGA for transmission permission control.

Pin #	Signal Name	Logic Level	Description
4	SDA	LVTTL-I/O	Two-Wire Serial Interface Data Line. Pull-up resistor required. <sup>(1)</sup>
5	SCL	LVTTL-I/O	Two-Wire Serial Interface Clock. Pull-up resistor required. <sup>(1)</sup>
6	Mod_ABS		Module Absent, connected to VeeT or VeeR in the module.
7	RS0	LVTTL-I	Rate Select 0, optionally controls SFP+ module receiver. Connects to FPGA. <sup>(2)</sup>
8	RX_LOS	LVTTL-O	Receiver Loss of Signal Indication (designated as RX_LOS in FC and Signal Detect in Ethernet). Open-drain output, which needs to be pulled up to VCC on the host side to instruct the SFP+ module to receive LOS alarms. RX_LOS needs to be connected to the FPGA. If the system needs to select a clock source, the LOS alarm will be monitored.
9	RS1	LVTTL-I	Rate Select 1, optionally controls SFP+ module receiver. Connects to FPGA. <sup>(2)</sup>
10	VeeR		Module Receiver Ground.
11	VeeR		Module Receiver Ground.
12	RD-	CML-O	Receiver Inverted Data Output.
13	RD+	CML-O	Receiver Non-Inverted Data Output.
14	VeeR		Module Receiver Ground.
15	VccR		Module Receiver 3.3 V Supply. <sup>(3)</sup>
16	VccT		Module Transmitter 3.3 V Supply. <sup>(3)</sup>
17	VeeT		Module Transmitter Ground.
18	TD+	CML-I	Transmitter Non-Inverted Data Input.
19	TD-	CML-I	Transmitter Inverted Data Input.
20	VeeT		Module Transmitter Ground.

## Differential Signals

The signal pair is LVDS, which requires AC coupling. The SFP+ module has integrated AC coupling capacitors. The 100  $\Omega$  termination resistor can be configured inside the FPGA. Therefore, the transceiver's differential signal for the SFP+ interface is connected directly to the differential interface of the FPGA.

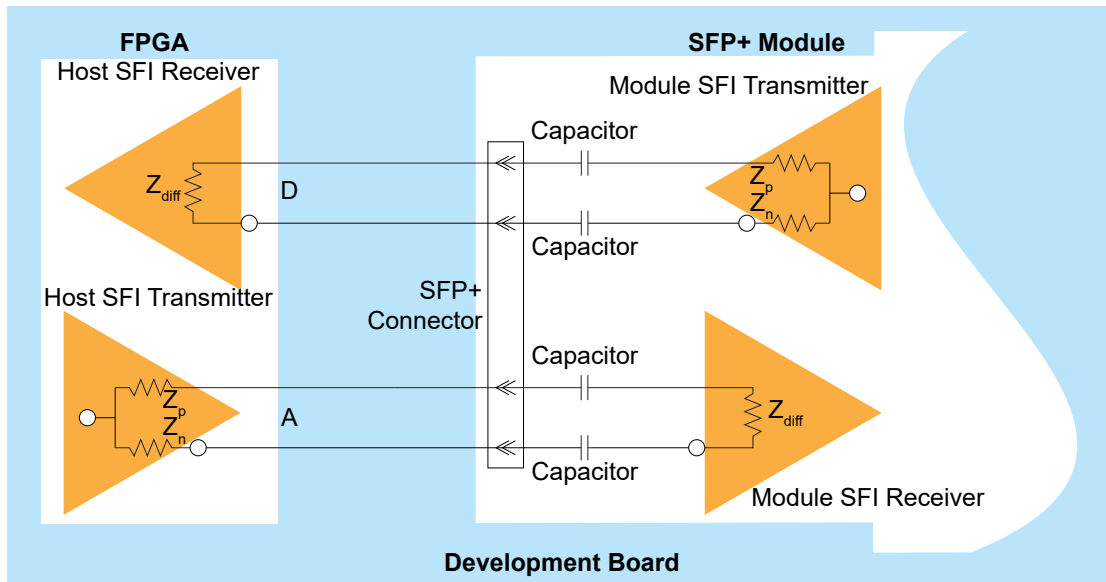
<sup>(1)</sup> Some SFP+ modules support reading the temperature of the optical module, which is useful when the optical interface power is relatively high. If there are multiple optical modules present, but the FPGA only has one set of I<sup>2</sup>C interfaces available, adding I<sup>2</sup>C buffer applies to ensure the reliability of I<sup>2</sup>C access.

<sup>(2)</sup> If RS0 and RS1 select GE modules, then the signal format of the SFP+ interface is SGMII. In this case, the FPGA's transceiver interface reference clock should be adjusted from 156.25 MHz of 10 G to 125 MHz of GE.

<sup>(3)</sup> Ferrite beads and a capacitor filter are recommended for supply noise reduction.

The following figure shows the transceiver interface connection of the SFP+ optical module.

Figure 7: SFP+ Interface Termination and AC Coupling



## Reference Clocks

Per the SFP+ optical interface block diagram, there are only two pairs of differential signals between the SFP+ optical module and the FPGA's transceiver interface. Nevertheless, the transceiver interface of the FPGA requires a reference clock for normal operation.

In 10G Base-R/KR mode, the reference clock frequency is 156.25 MHz. In SGMII mode, the reference clock frequency is 125 MHz.

The following table lists the typical electrical characteristics required of a 10G SFP+ interface reference clock.

Table 2: Reference Clock Typical Requirements for SFP+ Interface

Requirements	Condition	Minimum	Typical	Maximum	Unit
Reference Clock Frequency			156.25		MHz
Frequency Stability			<25		ppm
Jitter			<200		fs
Rise Time	20% ~ 80%	-	200	-	Ps
Drop Time	80% ~ 20%	-	200	-	Ps
Duty Cycle Requirements		40	50	60	%
Vpk-pk Voltage		250	-	2000	mV
Differential Input Impedance		-	100	-	Ohm ( $\Omega$ )

## PCIe Interface

PCIe v4.0 offers greater flexibility and bandwidth over its v3.0 predecessor, with a maximum transfer rate of 16 GT/s. The following table outlines the line code and maximum transfer rate for each PCIe generation.

**Table 3: PCIe Generation Comparison**

Generation	Line code		Max. Transfer Rate (per lane)
1.0	NRZ	8b/10b	2.5 GT/s
2.0			5.0 GT/s
3.0	NRZ	128b/130b	8.0 GT/s
4.0			16.0 GT/s

## Pin Definition

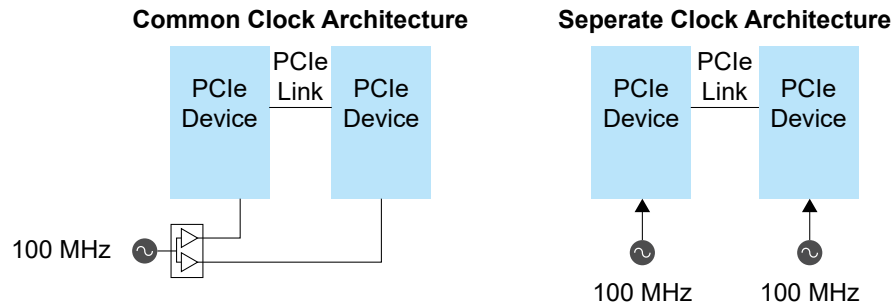
**Table 4: PCIe x4 Connector Pinout**

Pin #	Side B		Side A	
	Name	Description	Name	Description
1	+12 V	+12 V power	PRSNT1#	Hot-plug presence detected
2	+12 V	+12 V power	+12 V	+12 V power
3	+12 V	+12 V power	+12 V	+12 V power
4	GND	Ground	GND	Ground
5	SMNCLK	SMBus (System Management Bus) clock	JTAG2	TCK Clock input for JTAG interface
6	SMBDAT	SMBus (System Management Bus) data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3 V	+3.3 V power	JTAG5	TMS
9	JTAG1	TRST# (Test Reset) Resets the JTAG interface.	+3.3 V	+3.3 V power
10	+3.3 Vaux	+3.3 V auxiliary power	+3.3 V	+3.3 V power
11	WAKE#	Signal for link reactivation	PERST#	Fundamental reset
<b>Mechanical Key</b>				
12	CLKREQ#	Clock Request Signal	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, lane 0	REFCLK-	
15	PETn0	Transmitter differential pair, lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, lane 0
17	PRSNT2#	Hot-plug presence detected	PERn0	
18	GND	Ground	GND	Ground
<b>End of the x1 Connector</b>				
19	PETp1	Transmitter differential pair, lane 1	RSVD	
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, lane 2	GND	Ground

## PCIe Reference Clocks

The two main types of clock architecture in PCIe systems are common and separate reference clocks.

Figure 8: PCIe Clock Architecture



As the name suggests, in a common clock architecture the PCIe devices share the same PLL clock. This method is the most widely used clock architecture in PCIe systems. For PCIe Gen4 or below, the required frequency stability is  $\pm 300$  ppm.

The separate clock architecture use different clock sources for the host and endpoint devices. The frequency stability requirement is  $\pm 100$  ppm regardless of the system's bit rate. Both common and separate clock architectures support spread spectrum clocking (SSC) for reducing electromagnetic interference.

The jitter limit, shown in the following table, is specified according to PCIe generation.

Table 5: REFCLK Jitter Limit Requirements

PCIe Generation	REFCLK Phase Jitter Limit (ps RMS)
PCIe 1.1	86
PCIe 2.1	3.1
PCIe 3.1	1.0
PCIe 4.0	0.5

Additional AC and DC requirements for PCIe REFCLK are as shown in the following table:

Table 6: REFCLK Timing Requirements

Symbol	Parameter	100 MHz Input		Units	Notes
		Min.	Max.		
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	(†)(‡)
Falling Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	(†)(‡)
$V_{IH}$	Differential Input High Volatage	+150		mV	(†)
$V_{IL}$	Differential Input Low Volatage		-150	mV	(†)
$V_{CROSS}$	Absolute Crossing Point Voltage	+250	+550	mV	(*)

(\*) The measurement spec is for the waveform of a single-ended signal.

(†) The measurement spec is for the waveform of the differential signal.

(‡) Regarding the frequency stability of the reference clock, the clock accuracy requirements are different depending on the clock architecture.

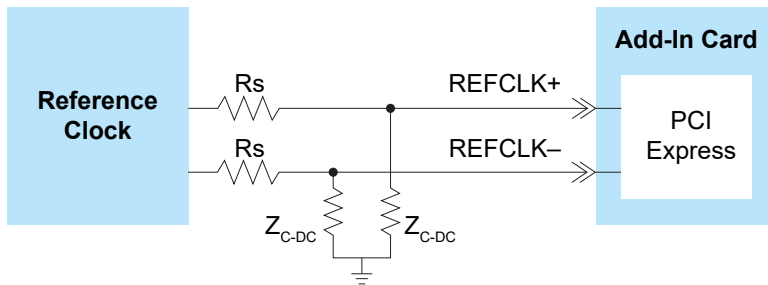
Symbol	Parameter	100 MHz Input		Units	Notes
		Min.	Max.		
V <sub>CROSS DELTA</sub>	Variation of V <sub>CROSS</sub> Over All Rising Clock Edges		+140	mV	(*)
V <sub>RB</sub>	Ring-Back Voltage Margin	-100	+100	mV	(†)
T <sub>STABLE</sub>	Time Before V <sub>RB</sub> is Allowed	500		ps	(†)
T <sub>PERIOD AVG</sub>	Average Clock Period Accuracy	-300	+2800	ppm	(†)
T <sub>PERIOD ABS</sub>	Absolute Period (including Jitter and Spread Spectrum Modulation)	9.847	10.203	ns	(†)
T <sub>CCJITTER</sub>	Cycle to Cycle Jitter		150	ps	(†)
V <sub>MAX</sub>	Absolute Maximum Input Voltage		+1.15	V	(*)
V <sub>MIN</sub>	Absolute Minimum Input Voltage		-0.3	V	(*)
Duty Cycle	Duty Cycle	40	60	%	(†)
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching		20	%	(*)
Z <sub>C-DC</sub>	Clock Source DC Impedance	40	60	Ω	(*)

The PCIe Controller accepts clock signals from both REFCLK0\_P/N and REFCLK1\_P/N.



**Note:** For computer applications, the main board has a reference clock for add-in cards on pin 13-14 on side A. The REFCLK is a 100-MHz HCSL clock.

Figure 9: PCIe Reference Clock Termination



**Note:** The default clock reference is REFCLK0. The clock multiplexer requires some clock toggling to switch from REFCLK0 to REFCLK1. For more details, please refer to the [Titanium PCIe® Controller User Guide](#).

For the reference clock measurement method, refer to the requirements in the following waveform diagrams:

Figure 10: Rise/Fall Edge for Differential Reference Clock

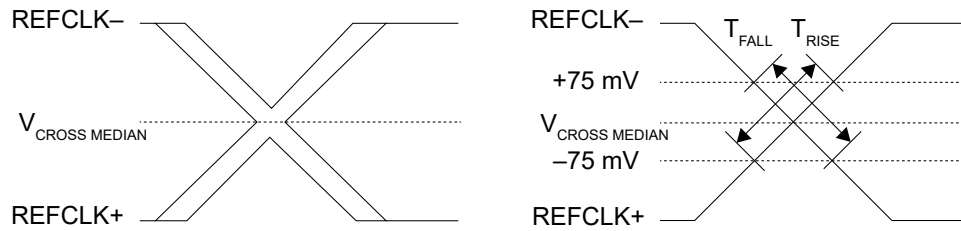


Figure 11: Rise/Fall Edge for Signal-Ended Reference Clock

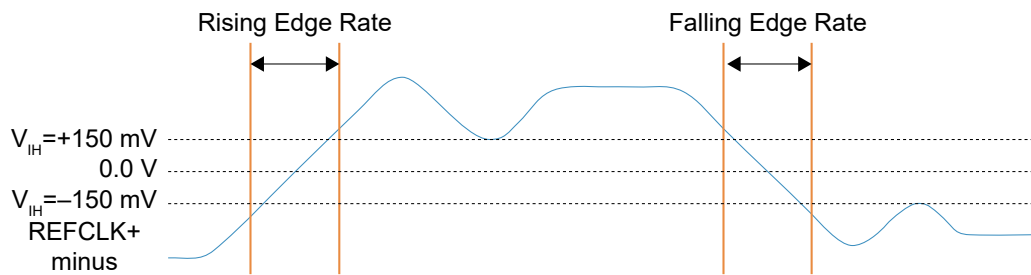


Figure 12: Period and Duty Cycle for PCIe Reference Clock

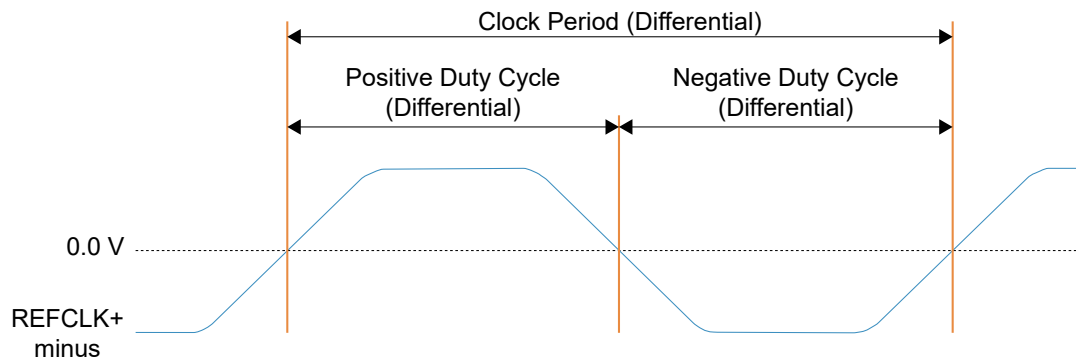
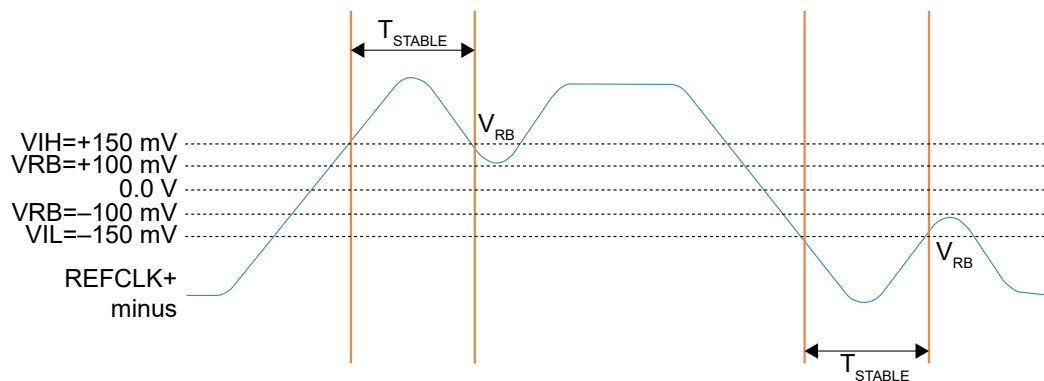


Figure 13: Ring Requirements for PCIe Reference Clock



### Reset Signals ( $PERST\_N$ )

The reset signal is used by the host device to indicate that the device power and reference clock are stable, and that link initialization is ready to begin. In Titanium and Topaz devices,

the PERST pin must connect to a dedicated pin, such as PERST\_Q0\_N or PERST\_Q2\_N, for proper operation.

## Implementing a Hot-Plug PCIe Interface

To implement the hot-plug features on PCIe add-in cards will require the mechanical support of the PRSNT1# and PRSNT2# pin connectors. These are the first and the most distant pins on the add-in card.

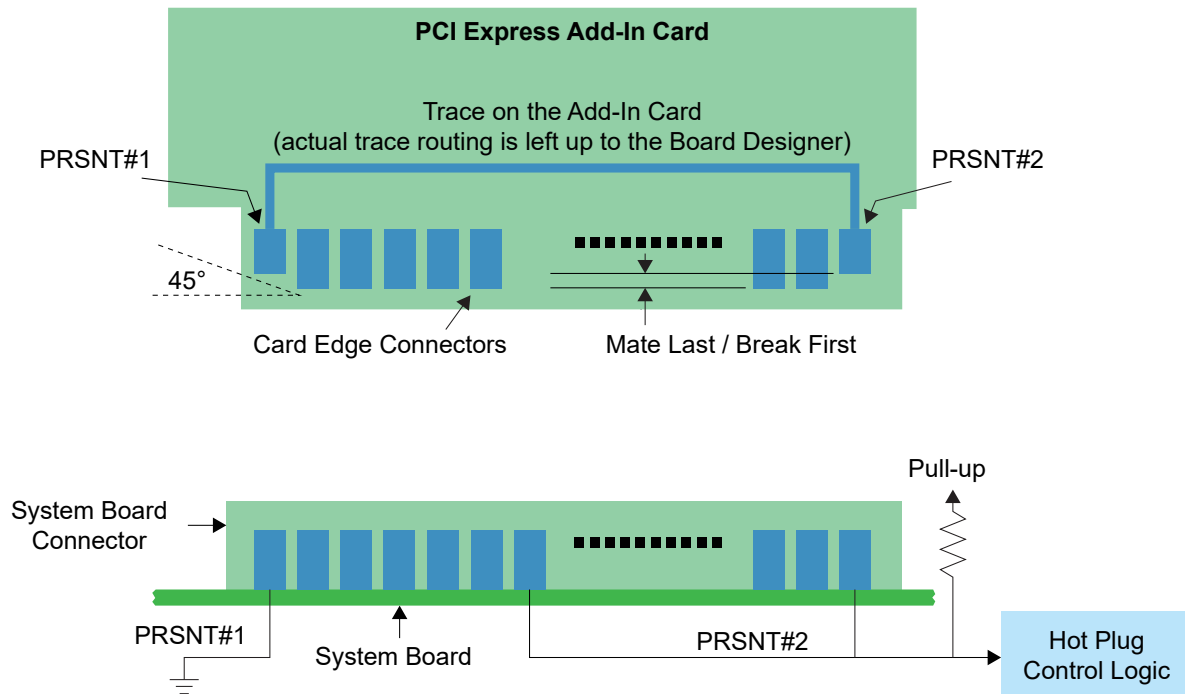


**Note:** For a x4 add-in card, PRSNT1# and PRSNT2# are mapped on A1 and B31, respectively.

On the PCB footprint, these are the shortest pins on the edge connector and the last signal connection during card insertion.

On the host board, if presence detection is supported, PRSNT1# must connect to ground and PRSNT2# must connect with a pull-up resistor; otherwise, both must be left unconnected. The following diagram illustrates hot-plug implementation.

Figure 14: PCIe Hot Plug

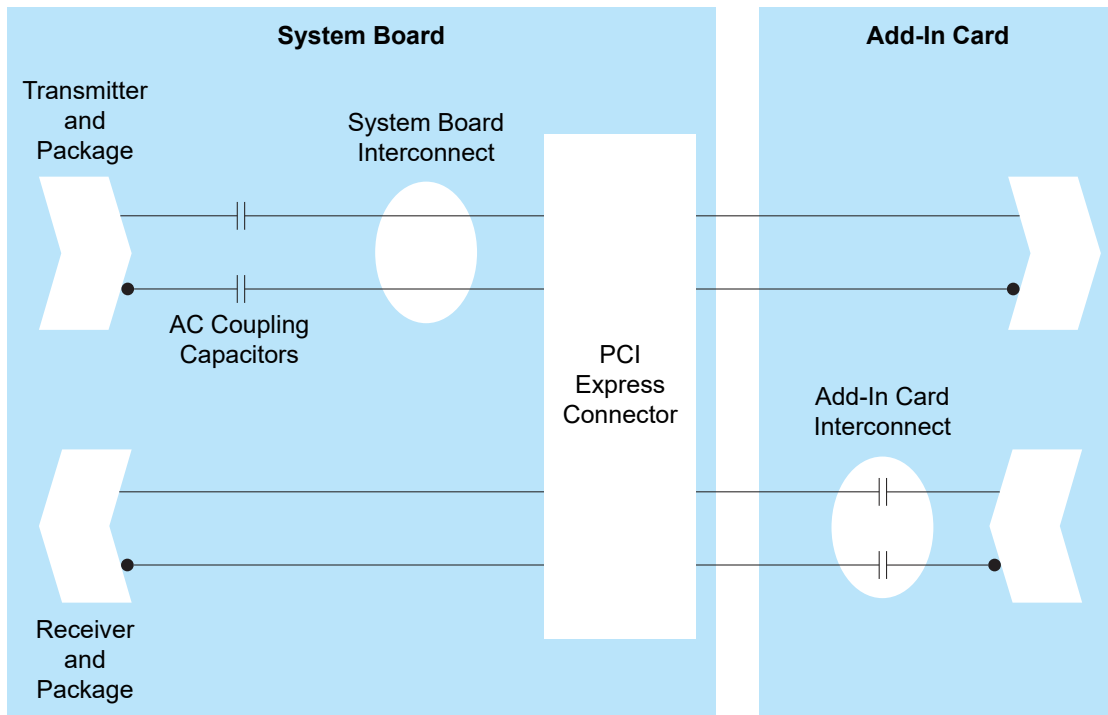


## PCIe Interface Differential Signals

According to the PCIe specification, the:

- PCIe interface differential signal uses AC coupling mode
- AC coupling capacitor is located on the TX side
- Capacitance size is 176 nF ~ 265 nF
- Conventional selection is 220 nF
- Recommended package is 0201

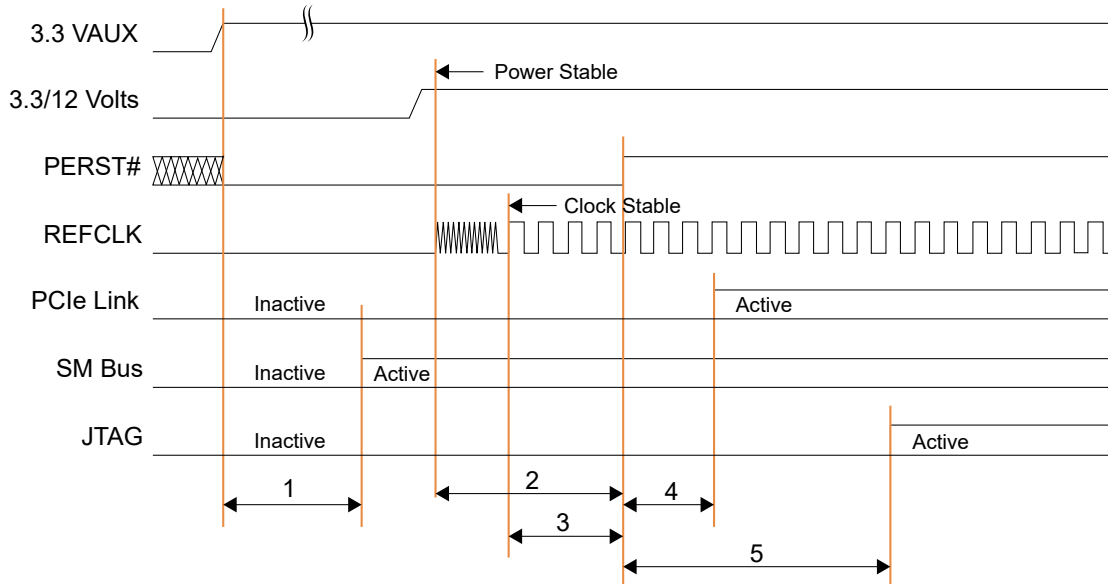
Figure 15: Differential Signal Connection for PCIe Interface



## Power Up Sequence

The PCIe endpoint device must follow the power-up sequence as described in the [Titanium PCIe® Controller User Guide](#).

Figure 16: Power-Up Sequence



### Notes:

- 3.3 VAUX stable to SM Buss driven (optional). If no 3.3 VAUX on platform, the delay is from 3.3 V stable.
- Minimum time from power rails within specified tolerance to PERST# inactive ( $T_{PVPERL}$ ).
- Minimum clock valid to PERST# inactive ( $T_{PERST-CLK}$ ).
- Minimum PERST# inactive to PCIe link out of electric idle.
- Minimum PERST# inactive to JTAG driven (optional).

## Boot-Up Timing Requirements

According to the PCIe specifications, the endpoint device must ensure that the board completes boot-up within 100 ms after PERST# deasserted. To this end, it is necessary to take into consideration the following design concerns:

- Overall power-rail start-up timing
- SPI, data width and data rate, configuration time
- Using PLL BL0 or BR0 for quad with an on-board oscillator as the PLL input clock source (depending upon Quad0/1 controller utilization).

For more information, please refer to the [Titanium PCIe® Controller User Guide](#).

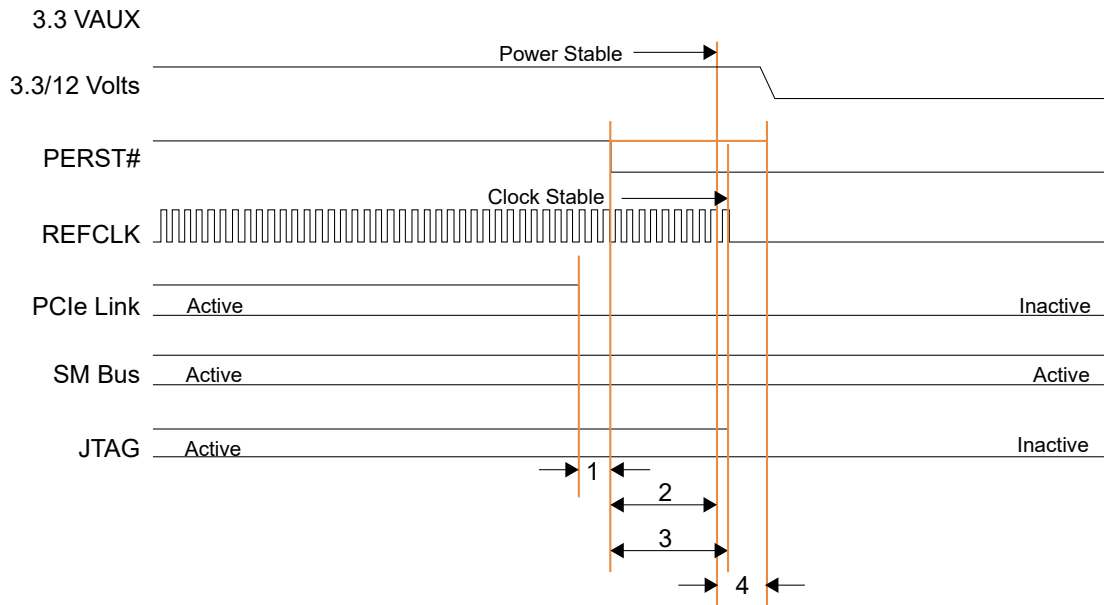
## Power-Down Sequence

The correct power-down sequence for the PCIe interface is as follows:

1. Before unplugging the AIC, the system must put the PCIe link into an inactive state.
2. The host asserts PERST#.
3. The system inactivates REFCLK and JTAG.

The following waveform illustrates the power down process.

Figure 17: Power-Down Sequence



Notes:

1. The PCIe link inactivates (Device in D3hot) prior to PERST# going active, except in the case of an unexpected power down.
2. PERST# goes active before the power connector is removed.
3. Clock and JTAG inactivate after PERST# goes active.
4. In the event of an unexpected power down, PERST# goes active TFAIL after power becomes unstable.

## Pre-Emphasis, De-Emphasis, and Equalization

During signal transmission, different frequency components experience varying degrees of attenuation leading to distortion in the received signal. To achieve a better waveform at the receiving end, it is essential to compensate for signal degradation. Common compensation techniques include pre-emphasis, de-emphasis, and equalization.

In high-speed signal transmission, high-frequency components are attenuated significantly more than low-frequency components, thus causing the transmission line to behave like a low-pass filter.

### Pre-Emphasis

Pre-emphasis involves boosting the signal's high-frequency components at the start of the transmission line to counteract the excessive attenuation they face during transmission. These high-frequency components are primarily found at the rising and falling edges of the signal. The pre-emphasis technique enhances the amplitude at these edges.

### De-Emphasis

The goal is to maintain a constant amplitude at the rising and falling edges while reducing the amplitude of the signal elsewhere. This approach offers several advantages, such as lower power consumption and reduced electromagnetic interference (EMI).

## Equalization

Equalization techniques can effectively address signal loss during transmission and improve overall signal quality. However, both pre-emphasis and de-emphasis techniques have their limitations; for example, they can inadvertently amplify high-frequency crosstalk, thereby exacerbating its impact. Equalization helps to mitigate these drawbacks. This technique functions as a high-pass filter, compensating for distorted pulses. An adaptive equalizer continuously adjusts its gain based on the actual digital signal transmitted, using an algorithm to respond to random channel changes. This adaptability ensures that the equalizer remains optimally configured, enhancing its ability to compensate for distortion.

# PCB Design Considerations

Several factors need to be considered in the design of your board. These factors include:

- Board material selection
- PCB stack up
- Impedance control
- Routing guidelines

## Board Material Selection

In high-frequency applications, the choice of board material is essential for ensuring optimal signal integrity, thermal management, and overall reliability. Materials with low dielectric constants and dissipation factors, high thermal stability, and good mechanical properties are essential for maintaining performance in high-speed electronic systems. Selecting the right material minimizes losses and enhances the efficiency of the circuit, thus making it a critical consideration in PCB design.

### *Dielectric Constant (Dk)*

The dielectric constant (Dk), or relative permittivity, is a measure of a material's ability to store electrical energy in an electric field relative to the vacuum. Dk is a critical property in the design and performance of electronic circuits, particularly in high-frequency applications, such as RF and microwave circuits. A lower Dk value (less than 4) is preferred as it helps reduce signal loss and maintain signal integrity. Medium Dk materials (around 4 to 10) offer a balance between cost and performance.

### *Dissipation Factor (Df)*

The dissipation factor (Df), also known as the loss tangent ( $\delta$ ), is a measure of how much energy from an electric field is lost as heat in a dielectric material. Df is a critical parameter in determining the efficiency and performance of electronic components, particularly in high-frequency applications. A low Df (less than 0.005) is essential for minimizing energy loss and heat generation, and is especially important in high-frequency scenarios. A medium Df (around 0.005 to 0.02) offers a balance between cost and performance.

### *Thermal Stability (Tg)*

The Glass Transition Temperature (Tg) represents the temperature threshold at which resin transforms from a solid state to rubbery fluid. High-frequency circuits can generate significant heat. Materials with high Tg can better withstand thermal cycling and maintain their properties, ensuring reliable operation over time. Tg is one of the important characteristics of PCB substrates, and is classified as:

- General Tg sheet: 130#-150#, such as KB-6164F (140#), S1141 (140#)
- Medium Tg sheet: 150#-170#, such as KB-6165F (150#), S1141 150 (150#)
- High Tg sheet: 170# and above, such as KB-6167F (170#), S1170 (170#)

## Other Considerations

Other PCB material properties, such as Conductive Anodic Filament (CAF), Thermal Conductivity (TC), Coefficient of Thermal Expansion (CTE), etc., must be considered in terms of the manufacturing of high-density, high-power applications.

**Table 7: Examples of PCB Materials**

Type	Dk (1GHz)	Df (1GHz)	Price	Reference
Resin	3.6	0.025	Low	TU768/TU752/IT180A
PPE	2.45	0.007	High	Megtron6/TU883
PTPE	2.1	0.0004	Very high	RO3000 Series

## PCB Stack Up

Due to the growth in the demand for more compact PCBs, the issue of design stack up has become increasingly important. Good PCB management also helps reduce EMI and improve signal integrity. Here are some rules for stack-up design:

- If the high-speed signal goes through the surface layer, the adjacent layer needs a complete ground plane.
- If the high-speed signal goes to the inner layer, the upper/lower adjacent layers should be placed with a complete ground plane.
- The power plane must be adjacent to the full ground plane layer and tightly coupled.
- TX and RX signals for high-speed differential signals should ideally be placed in different layers.
- From the perspective of EMC, a high-speed clock and high-speed parallel signal avoids surface wiring.
- Stackups need to be cost-effective.

According to the PCIe CEM specifications, the overall thickness of a PCIe card should be 1.57 mm.

## Impedance Control

Target trace impedance for PCIe interfaces should follow the recommendations below. The tolerance for manufacturing should be kept at  $\pm 5\%$ .

PCIe Generation	Single-End Impedance	Differential Impedance
Gen1	50 $\Omega$	100 $\Omega$
Gen2	50 $\Omega$	100 $\Omega$
Gen3	50 $\Omega$ or 42.5 $\Omega$	100 $\Omega$ or 85 $\Omega$
Gen4	42.5 $\Omega$	85 $\Omega$

## Routing Guidelines

In the course of designing your PCB, you must observe the following routing guidelines:

### *Microstrip vs Stripline*

Microstrip traces are located on the surface layers while stripline is fully confined, meaning that it has minimal radiation and resistance to interference. There are no strict rules regarding which way the high-speed signals need to be routed. Engineering should make the determination between microstrip and stripline routine according to the use case scenario. The following topics compare the advantages and disadvantages of microstrip vs stripline.

#### Microstrip

- Consists of a signal conductor strip and references to the adjacent ground plane with a layer of dielectric separation.
- Structure is simple, cost effective, and does not incur vias if interlayer routing is avoided. This strategy reduces the parasitic capacitance and inductance from via structure in high frequency applications. It also avoids signal reflection caused by via stubs.
- Reference plane is one-sided if the dielectric constant is less than the stripline, meaning that the transmission line delay is smaller and achievable for higher speed propagation.
- Microstrips are subject more interference as they are located on the surface layers.

#### Stripline

- Consists of an inner signal conductor strip sandwiched between two parallel reference planes (normally ground planes). These shield the signal and provide good EMC protection. However, fabrication complexity increases with the number of stack-up layers.
- Vias are required when traces change layers from top/bottom to inner. Through-hole vias introduce via stubs, which can be a source of signal reflection. Using blind or buried vias, or back drilling, can eliminate this issue, but increases production costs.

### *High-Speed Differential Trace Recommendations*

The following recommendations are provided to ensure the quality of high-speed differential traces.

## Trace Length

The trace length budget for add-in cards is a maximum of 101.6 mm, and with a maximum width of approximately 0.127 mm. Differential pairs are required to maintain equal width throughout the board.

## Spacing

The spacing between P and N wires of the differential pairs is determined by the design impedance according to line width, copper thickness, PCB material, and lamination. The spacing should be kept constant throughout, from the main chip to the edge connector. For example, if the clock signal width is  $\times 1$ , the distance between the clock signal and other signals should be consistent at  $\times 5$  spacing.

## Skew Matching

The intra-pair skew requirement for high-speed differential pairs is  $< 0.127$  mm. There are no inter-pair skew requirements in the PCIe specification.

## Bending

Round bending is recommended to maintain the continuity of impedance; however,  $45^\circ$  corners are acceptable. Do not use right-angle bends.

## Other Routing Recommendations

Place TX and RX signals in different layers. Differential signal routing must be kept away from crystal oscillators, DC modules, magnetic components, and so on.

## PCIe v4.0 Routing Guide

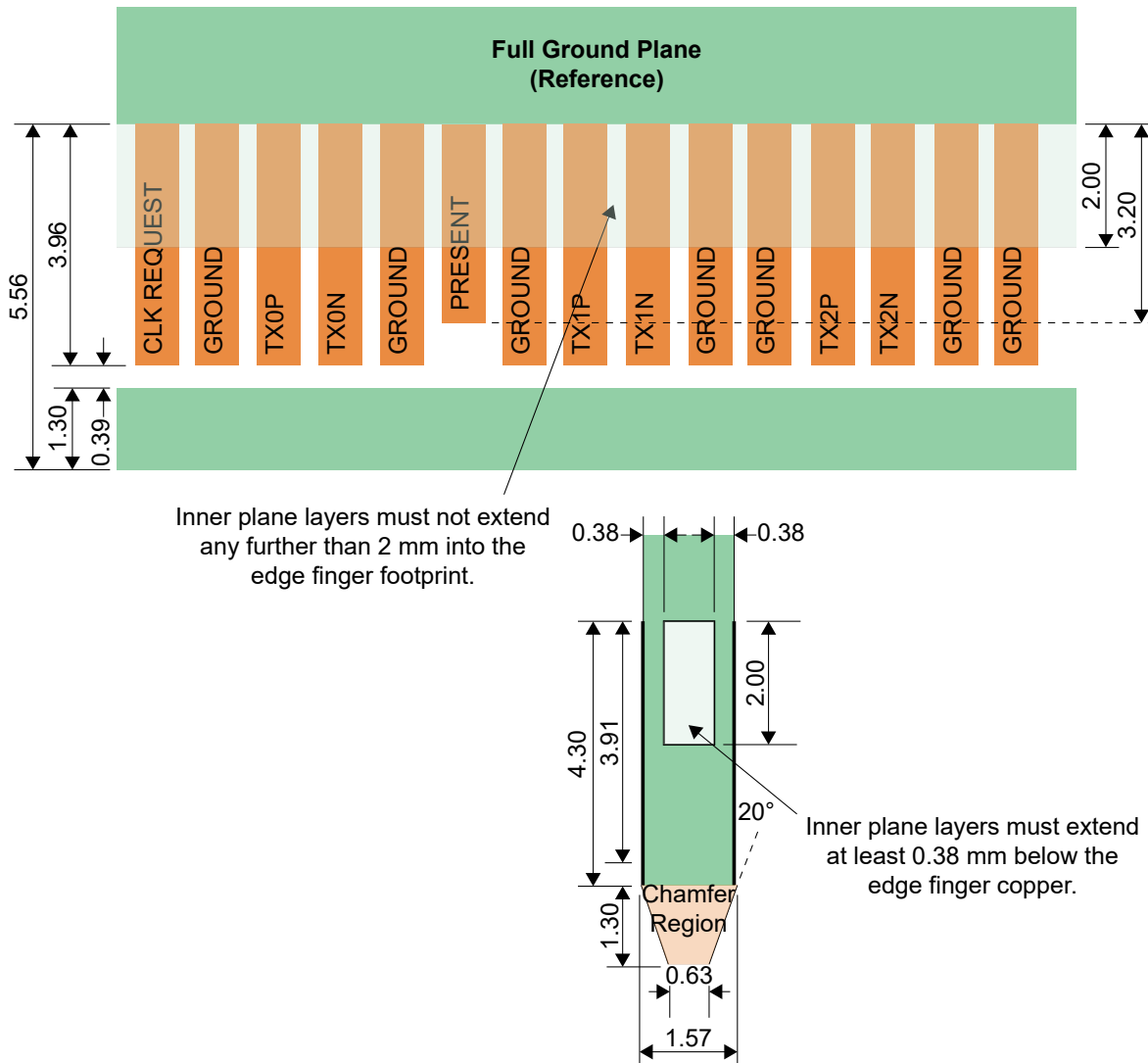
In addition to the common routing requirements for differential signals, it is also necessary to comply with the following PCIe v4.0 specifications:

### PCIe v4.0 Edge Card Connector Reference Plane

Per the PCIe v4.0 specifications, there is no inner conductor within 381 microns below the edge card connector, including no GND plane or power plane. It is recommended that the inner layer be more than 381 microns, and the GND plane placed to prevent crosstalk between TX and RX. Refer to the following diagram for details:

Figure 18: PCIe v4.0 Edge Card Connector Reference Plane Schematic

All dimensions in millimeters



### PCIe Edge Card Connector Length

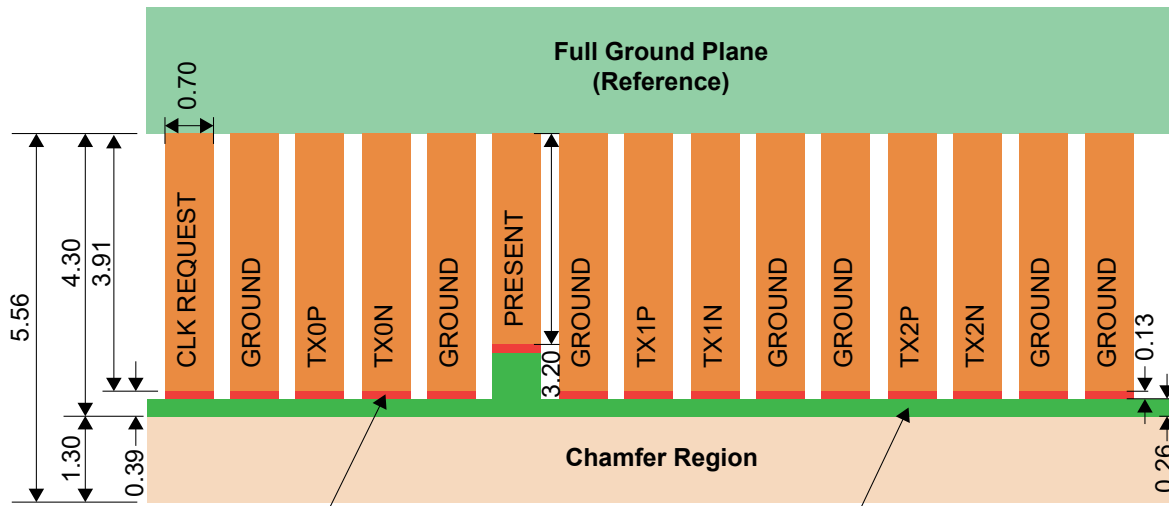
The length of the edge card connector is 3.91 mm, and the entire length (including the chamfer area) of the edge card connector is 5.6 mm. The space between the edge card connector area and the chamfer area is 0.39 mm, which is less than in Gen 1.

A small amount of residual surface metal is allowed within the 0.13 mm area beyond the lower end of the edge card connector.

The PRSNT1# or PRSNT2# pins should be 3.2 mm in length, while the non-functional PRSNT2# edge card connector can be either 3.2 mm or 3.91 mm long.

Figure 19: PCIe v4.0 Edge Card Connector Reference Plane Schematic

All dimensions in millimeters



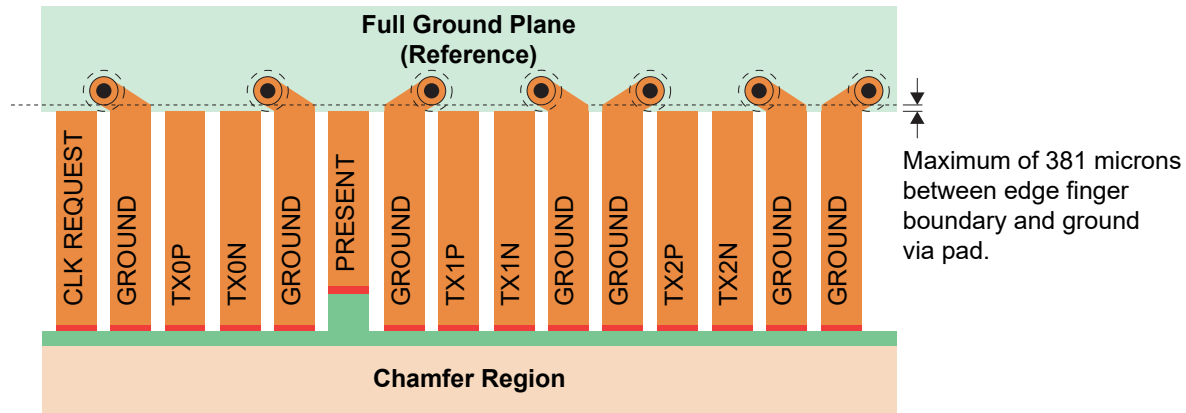
Some surface metal is permitted in the 0.13 mm high zone beyond the edge fingers.

The first 0.26 mm above the chamfer is free of all surface metal.

## Ground Hole Requirements

The ground hole of the edge card connector must be distributed in the middle of the adjacent pins of the edge card connector so as to reduce the interference of the signal outlet. From the top edge of the edge card connector to the bottom edge of the GND vias should not exceed 127 microns. The width of the traces connected to the GND via and GND pin must be greater than or equal to the diameter of the via pad to minimize ground inductance. The front and back GND pins of edge card connector can share GND vias.

Figure 20: PCIe 4.0 Edge Card Connector Via Requirements



## Merging Edge Card Connector GND Vias

Edge card connector GND pins are adjacent to each other, with the GND vias connected to the GND pin connected together. The GND holes can also be shared on both sides.

## Revision History

Date	Version	Description
February 2026	1.2	Updated <b>PMA Direct</b> on page 3 with AC coupling requirements. (DOC-2871)
July 2025	1.1	Updated <b>PMA Direct</b> on page 3 with RX insertion loss guidelines. (DOC-2619)
March 2025	1.0	Initial Release.