



HyperRAM IP Core 2025.2 Update FAQ

November 2025

- HyperRAM controller IP supported RAM operating frequencies up to 200 MHz before the Efinity 2025.2 release
- In Efinity 2025.2, Efinix updated IP **version 6.12** to support 250-MHz operating clock for Ti60F100S3F2 and Ti35F100S3F2 non-L grade devices.
 - Ti60F100S3F2 with date code before 2236 can only support up to 200 MHz
 - Ti35F100S3F2 with date code before 2236 can only support up to 200 MHz

- Customer Advisory for the update ([ADV-2511-001](#))
- Updated HyperRAM controller IP document ([v3.9](#))
- [Previous HyperRAM controller IP document](#) (v3.8)

Q1. For hardware compatibility, will the new IP have different requirements for hardware design?

A1. No, the HyperRAM is in the package (SIP). Only Ti60F100S3F2 with date codes on or after 2236 (and Ti35F100S3F2 with date codes on or after 2236) can support 250 MHz clocks. Others are still running up to 200 MHz.

Q2. On RTL compatibility, is the user interface such as signals and timing different from the old version?

A2. Signals will remain backward compatible. For 250-MHz performance, user needs to update the interface timing to meet the higher performance (250 MHz clock).

Q3. Is there any resource utilization change?

A3. There are new features added in the new IP revision to support Dynamic Configuration, Hybrid Sleep and Deep Power Down, and On-Demand Calibration. However, the impact on resource usage is minimal (about 15 FFs and 18 LUTs additional).

Q4. Does the user need to change any Interface Designer settings?

A4. The update is only applied for rules. There are no new parameters/settings in the Interface Designer.