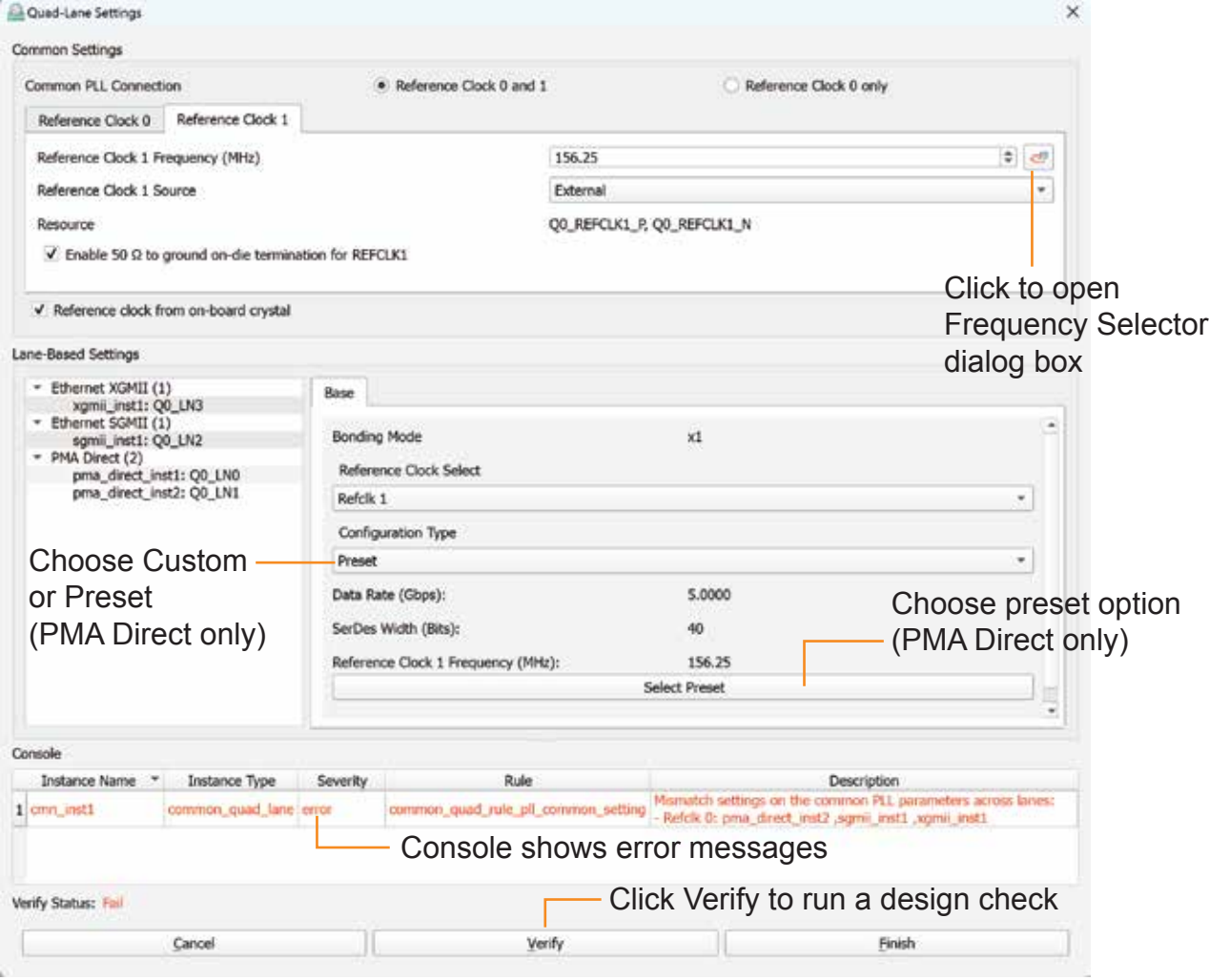
Quad-Lane Settings
Common Settings
Common PLL Connection
Reference Clock 0 and 1
Reference Clock 0 only
Reference Clock 0
Reference Clock 1
Reference Clock 1 Frequency (MHz)
156.25
Reference Clock 1 Source
External
Resource
Q0_REFCLK1_P, Q0_REFCLK1_N
Enable 50 Ω to ground on-die termination for REFCLK1
Reference clock from on-board crystal
Click to open Frequency Selector dialog box
Lane-Based Settings
Ethernet XGMII (1)
xgmii_inst1: Q0_LN3
Ethernet SGMII (1)
sgmii_inst1: Q0_LN2
PMA Direct (2)
pma_direct_inst1: Q0_LN0
pma_direct_inst2: Q0_LN1
Base
Bonding Mode
x1
Reference Clock Select
Refclk 1
Configuration Type
Preset
Data Rate (Gbps):
5.0000
SerDes Width (Bits):
40
Reference Clock 1 Frequency (MHz):
156.25
Select Preset
Choose Custom or Preset (PMA Direct only)
Choose preset option (PMA Direct only)
Console
Instance Name
Instance Type
Severity
Rule
Description
1
cmn_inst1
common_quad_lane
error
common_quad_rule_pll_common_setting
Mismatch settings on the common PLL parameters across lanes:
- Refclk 0: pma_direct_inst2 ,sgmii_inst1 ,xgmii_inst1
Console shows error messages
Verify Status: Fail
Click Verify to run a design check
Cancel
Verify
Finish