

The screenshot displays the Efinity Interface Designer interface with the following components and callouts:

- 1**: Design Explorer search bar.
- 2**: Block Summary table.
- 3**: Block Editor settings for the selected block.
- 4**: File menu.
- 5**: Design menu.
- 6**: Show/Hide Resource Assigner icon.
- 7**: Block tools (add, delete).
- 8**: Design Explorer expand/collapse icons.
- 9**: I/O Banks (5) folder in Design Explorer.
- 10**: Package Planner icon.

Block Summary Table:

Property	Value
1 Instance Name	Oclk_out
2 GPIO Resource	GPIOR_13
3 Mode	clkout
4 I/O Standard	3.3 V LVTTTL / LVCMOS
5 Unused State	NA
6 Alternate Connection	None
7 Features	None
8 Clock Region	R1
9 I/O Bank	2A
10 Pad	GPIOR_13
11 Package Pin	D6
12 Clkout Output	
13 Clock Pin Name	Oclk
14 Clock Is Inverted	false
15 Drive Strength	1

Block Editor Settings:

- Oclk_out
- Mode: clkout
- I/O Standard: 3.3 V LVTTTL / LVCMOS
- Output: Pin Name (empty), Constant Output: none, Register Option: none, Drive Strength (1-weakest, 4-strongest): 1, Enable Slew Rate:
- Output Clock

Notes:

1. The Design Explorer shows the interface blocks in your design. They are organized by block type.
2. The block summary shows the settings for the block selected in the Design Explorer.
3. Use the Block Editor to add or change settings for the interface block.
4. You can import or export GPIO resource assignments using a **.csv** or **.isf** file.
5. Use the project management tools to perform design checks, view reports, generate constraints, etc.
6. Click Show/Hide Resource Assigner to toggle a tabular view of assignments.
7. Use the block tools to add or delete blocks and buses.
8. Expand or collapse the Design Explorer folders.
9. The number in parentheses shows the number of used blocks.
10. The Package Planner lets you see the pins and assignments graphically.